Feasibility and Simulation Study of DC hybrid circuit breakers

by

Shang Yang

A thesis submitted in conformity with the requirements
for the degree of Master of Applied Science
Graduate Department of Electrical Engineering
University of Toronto

Abstract

Feasibility and Simulation Study of DC hybrid circuit breakers

Shang Yang
Master of Applied Science
Graduate Department of Electrical Engineering
University of Toronto
2014

Interruption of DC is more challenging than that of AC because of the absence of DC zero-crossings. This thesis proposes an alternative counter-voltage (ACV) DC hybrid circuit breaker (DC-HCB). This DC-HCB can interrupt the DC up to 5 kA with the source voltage of up to 1 kV and it can meet the general requirements i.e., interrupting the DC within 5ms, and limiting over-voltages due to the CB operation. The existing/investigated DC circuit breakers, i.e., active mode DC-HCB and the traditional counter-voltage (TCV) DC-HCB are also investigated and compared with the proposed DC-HCB. The investigations are based on the time-domain simulation studies in the PSCAD/EMTDC. The studies show that the ACV DC-HCB is the preferred option to both the existing DC-HCBs. The main features of the proposed ACV DC-HCB include lower capacitance in the commutation path and the need for a smaller dielectric strength for the primary-path circuit breaker.

Contents

1 Introduction **1**

1.1 Problem Statement 1

1.2 Literature Review 2

1.2.1 DC Interruption Techniques 3

1.2.2 DC-CB Types 5

1.3 Thesis Objective 7

1.4 Thesis layout 8

2 Principles of Operation of DC-HCBs **10**

2.1 Introduction 10

2.2 DC-CB Configurations 10

2.2.1 Configuration I: Active Mode DC-HCB 10

2.2.2 Configuration II: DC-HCB Based on MOV 13

2.2.3 Configuration III: Counter-Voltage DC-HCB 15

2.2.4 Configuration IV: Proposed Counter-Voltage DC-HCB 17

2.3 Comparison of DC-CB Configurations 19

2.4 Study System 21

2.5 Methodology 21

2.6 Conclusion 22

3 Electric Arc Model **23**

3.1 Introduction 23

3.2 Arc Phenomenon Under AC and DC 24

3.2.1 Electric Arc Fundamentals 24

3.2.2 Interruption of AC 25

3.2.3 Interruption of DC 26

3.3 Arc Models 27

3.3.1 AC Arc Model 28

3.3.2 DC Arc Model . . . 31
3.4 Conclusions . . . 39

4 Analysis and Simulation of Active Mode DC-HCB 41
4.1 Introduction . . . 41
4.2 Analysis of Active Mode DC-HCB . . . 42
4.2.1 Time Intervals for Fault Current Interruption . . . 44
4.2.2 Dynamic Performance of the Active Mode DC-HCB . . . 50
4.3 Impact of DC arc . . . 55
4.4 Conclusion . . . 59

5 Analysis and Simulation of Counter-Voltage DC-HCBs 60
5.1 Introduction . . . 60
5.2 Analysis of Counter-Voltage DC-HCBs . . . 60
5.2.1 Analysis of the TCV DC-HCB . . . 61
5.2.2 Analysis of the ACV DC-HCB . . . 67
5.3 Dynamic Performance of Counter-Voltage DC-HCBs . . . 77
5.3.1 Dynamic Performance of TCV DC-HCB . . . 83
5.3.2 Dynamic Performance of ACV DC-HCB . . . 84
5.3.3 Discussion . . . 85
5.4 Impact of DC arc . . . 85
5.5 Conclusion . . . 87

6 Performance Evaluation of the Proposed DC-HCB 89
6.1 Introduction . . . 89
6.2 Comparison of Active Mode DC-HCB with ACV DC-HCB . . . 89
6.3 Performance of the ACV DC-HCB in the DC Study System . . . 92
6.4 Performance Evaluation of the ACV DC-HCB . . . 95
6.4.1 LVDC Study System . . . 95
6.4.2 Performance Evaluation . . . 96
6.5 Conclusion . . . 103

7 Conclusions and Future Work 104
7.1 Future work . . . 105

Bibliography 105

List of Tables

2.1 Parameters of a typical DC cable 21

3.1 Parameter values for Mayr and Cassie arc models 29
3.2 Paukert's empirical arc voltages 33
3.3 Paukert's empirical arc resistances 33
3.4 Three cases of DC arc model simulations 36

4.1 42
4.2 Comparisons of analytical results (Section 4.2) with simulation results (Section 4.3) 56

5.1 61
5.2 69
5.3 PSCAD/EMTDC simulation results of the TCV DC-HCB 86
5.4 PSCAD/EMTDC simulation results of the ACV DC-HCB 86

6.1 PSCAD-based simulation results of the active mode DC-HCB 91
6.2 PSCAD/EMTDC simulation results of the ACV DC-HCB 92
6.3 Analytical results of the ACV DC-HCB (1) 93
6.4 Analytical results of the ACV DC-HCB (2) 93
6.5 PSCAD simulation results of the ACV DC-HCB (1) 94
6.6 PSCAD simulation results of the ACV DC-HCB (2) 95
6.7 System Parameters of the LVDC study system model 96
6.8 Circuit Parameters of the ACV DC-HCB in LVDC study system model . 98

List of Figures

1.1 A structure of the passive mode DC-MCB 3

1.2 A structure of the active mode DC-HCB 3

1.3 A structure of counter-voltage topology DC-HCB 4

1.4 (a) A DC-SSCB paralleling a non-linear resistor, and (b) a DC-SSCB with a freewheeling diode 5

1.5 Circuit diagram of the DC-SSCB circuit 6

1.6 Basic configuration of the ultra-fast contact opening HCB 7

1.7 A structure of the proposed alternative counter voltage DC-HCB 8

1.8 Thesis layout 9

2.1 A basic configuration of the active mode DC-HCB 11

2.2 Fault current interruption process of Configuration I (FCZ= First Current Zero-crossing), (a) line current I_S, (b) current through the MCB I_B, (c) commutation current path I_c, and (d) voltage of the commutation capacitor V_C. 12

2.3 A basic configuration of the DC-HCB using a MOV 13

2.4 Fault current interruption process of Configuration II, (a) line current I_S, (b) current through the MCB I_B (c) commutation current path I_C (d) current through the MOV I_{MOV}, and (e) voltage across the MCB V_m. . . 14

2.5 A basic configuration of counter-voltage DC-HCB 15

2.6 Fault current interruption process of Configuration III, (a) line current I_c, (b) current through the MCB I_B, (c) commutation current path I_C, and (d) voltage of the commutation capacitor V_c. 16

2.7 A basic structure of proposed counter-voltage DC-HCB 17

2.8 Fault current interruption process of Configuration IV, (a) line current I_S, (b) current through the MCB I_C, (c) main commutation current path I_{com}, (d) primary commutation current path I_{CP}, (e) secondary commutation current path I_{CS}, (f) voltage of the primary commutation capacitor V_{CP}, and (g) voltage of the secondary commutation capacitor V_{CS}. 18
2.9 The structure of the LVDC distribution network 21

3.1 Voltage-current characteristic of an electric arc 24
3.2 Voltage distribution of high pressure arc column 25
3.3 Two cases of AC interruption 26
3.4 Two cases of DC system, (a) Case A: DC circuit without a system inductor, and (b) Case B: DC circuit with a system inductor 27
3.5 Study system for the AC arc model 30
3.6 Behavior of the Mayr arc model when CB opens at the current zero-crossing instant, (a) arc voltage of Mayr arc model (Case A), and (b) arc current of Mayr arc model (Case A). 30
3.7 Behavior of the Mayr arc model when CB opens at the maximum (peak) current, (a) arc voltage of Cassie arc model (Case B), and (b) arc current of Cassie arc model (Case B). 31
3.8 V-I characteristic for vertical arcs burning against aluminium electrodes (Stokes and Oppenlander) [1] 33
3.9 Paukert's empirical arc resistance versus arc current ranged from 10 to 300A with different length of electrode gap 34
3.10 A study system of the DC arc model 36
3.11 DC arc resistance when the dielectric strength of the contacts gap is small, (a) voltage of system inductor (Case A), (b) arc voltage of DC arc model (Case A), (c) arc resistance of DC arc model of Case A, and (d) arc current of DC arc model (Case A). 37
3.12 DC arc resistance with the minimum dielectric strength of the contacts gap, (a) voltage of system inductor (Case B), (b) arc voltage of DC arc model (Case B), (c) arc resistance of DC arc model of Case B, and (d) arc current of DC arc model (Case B). 38
3.13 DC arc resistance with the much large electrode gap, (a) voltage of system inductor (Case C), (b) arc voltage of DC arc model (Case C), (c) arc resistance of DC arc model of Case C, and (d) arc current of DC arc model (Case C). 39

4.1 Circuit configuration of an active mode DC-HCB 42
4.2 The interrupting process of active mode DC-HCB when the MCB opens at the second current zero-crossing (SCZ), (a) line current (I_S), (b) current through the MCB (I_B), (c) commutation current path (I_C), and (d) commutation capacitor voltage (V_c). 43
4.3 First time interval for the fault current interruption 44
4.4 Second time interval for the fault current interruption 45
4.5 Third time interval for the fault current interruption 46
4.6 Representation of the system of Fig 4.5 46
4.7 Fourth time interval for the fault current interruption 48
4.8 Fifth time interval for the fault current interruption 50
4.9 The total energy stored in the commutation capacitor, as a function of commutation capacitance and the final capacitor voltage 51
4.10 Case A, (a) C_c VS V_{cf} when interrupting at the FCZ or at the SCZ, (b)C_c VS TIT when interrupting at the FCZ or at the SCZ, (c) C_c VS I_{cmax} when interrupting at the FCZ or at the SCZ, and (d) C_c VS W_{ab} when interrupting at the FCZ or at the SCZ. 52
4.11 Case B, (a) L_T VS V_{cf} when interrupting at the FCZ or at the SCZ, (b)L_T VS TIT when interrupting at the FCZ or at the SCZ, (c) L_T VS I_{cmax} when interrupting at the FCZ or at the SCZ, and (d) L_T VS W_{ab} when interrupting at the FCZ or at the SCZ. 53
4.12 Case C, (a) V_{pre} VS V_{cf} when interrupting at the FCZ or at the SCZ, (b)V_{pre} VS TIT when interrupting at the FCZ or at the SCZ, (c) V_{pre} VS I_{cmax} when interrupting at the FCZ or at the SCZ, and (d) V_{pre} VS W_{ab} when interrupting at the FCZ or at the SCZ. 54
4.13 Case D, (a) I_{St} VS V_{cf} when interrupting at the FCZ or at the SCZ, (b)I_{St} VS TIT when interrupting at the FCZ or at the SCZ, (c) I_{St} VS I_{cmax} when interrupting at the FCZ or at the SCZ, and (d) I_{St} VS W_{ab} when interrupting at the FCZ or at the SCZ. 55
4.14 Simulation waveforms of the active mode DC-HCB of the FCZ interruption when K_a is 178.2, (a) I_s vs t, (b) I_B vs t, (c) I_c vs t, and (d) V_c vs t. . . 57
4.15 Simulation waveforms of the active mode DC-HCB of the FCZ interruption when K_a is 178.2, (a) I_s vs t, (b) I_B vs t, (c) I_c vs t, and (d) V_c vs t. . . 58

5.1 Configuration of a TCV DC-HCB 61

5.2 The interruption process of the TCV DC-HCB, (a) line current (I_S) (b) current through the MCB (I_B), (c) commutation current path (I_C), and (d) commutation capacitor voltage (V_c). 62
5.3 Circuit configuration of the TCV DC-HCB during the first time interval . 63
5.4 Circuit configuration of the TCV DC-HCB during the second time interval 63
5.5 Circuit configuration of the TCV DC-HCB during the third time interval 65
5.6 Circuit configuration of the TCV DC-HCB during the fourth time interval 67
5.7 Circuit configuration of the ACV DC-HCB 67
5.8 The interruption process of ACV DC-HCB, (a) line current (I_S), (b) current through the MCB (I_B), (c) main commutation current (I_{com}), (d) primary commutation current (I_{cp}), (e) secondary commutation current (I_{cs}), (f) primary commutation capacitor voltage (V_{cp}), and (g) secondary commutation capacitor voltage (V_{cs}). 68
5.9 ACV DC-HCB circuit configuration during the first time interval 69
5.10 ACV DC-HCB circuit configuration during the secondary time interval . 70
5.11 ACV DC-HCB circuit configuration during the third time interval 70
5.12 ACV DC-HCB circuit configuration during the fourth time interval . . . 71
5.13 ACV DC-HCB circuit configuration during the fifth time interval 72
5.14 Representation of the system of Fig 5.13 73
5.15 ACV DC-HCB circuit configuration during the sixth time interval 74
5.16 Representation of the system of Fig 5.15 75
5.17 ACV DC-HCB circuit configuration during the seventh time interval . . . 76
5.18 Effect of V_{pre} and C_c on the CB performance of TCV DC-HCB (Case A), (a) V_{pre} VS W_T, (b) V_{pre} VS V_{cf}, (c) V_{pre} VS TIT, (d)C_c VS W_T, (e)C_c VS V_{cf}, and (f)C_c VS TIT. 78
5.19 Effect of I_{St} and L_T on the CB performance of TCV DC-HCB (Case B), (a) I_{St} VS W_T, (b) I_{St} VS V_{cf}, (c) I_{St} VS TIT, (d)L_T VS W_T, (e)L_T VS V_{cf}, and (f)L_T VS TIT. 79
5.20 Effect of C_{com} on the CB performance of ACV DC-HCB (Case I), (a) C_{com} VS TIT, (b)C_{com} VS TIT with number of switching, (c) C_{com} VS W_T, and (d)C_{com} VS W_T with number of switching. 80
5.21 Effect of V_{max} on the CB performance of ACV DC-HCB (Case II), (a) V_{max} VS TIT, (b)V_{max} VS TIT with number of switching, (c) V_{max} VS W_T, and (d) V_{max} VS W_T with number of switching. 81

5.22 Effect of I_{St} on the CB performance of ACV DC-HCB (Case III), (a) I_{St} VS TIT, (b)I_{St} VS TIT with number of switching, (c) I_{St} VS W_T, and (d) I_{St} VS W_T with number of switching. 82

5.23 Effect of L_T on the CB performance of ACV DC-HCB (Case IV), (a) L_T VS TIT, (b)L_T VS TIT with number of switching, (c) L_T VS W_T, and (d) L_T VS W_T with number of switching. 83

6.1 Circuit configuration of active mode DC-HCB 90

6.2 Circuit configuration of Alternative Counter-voltage(ACV) DC-HCB . . 90

6.3 Configuration of the LVDC distribution network 96

6.4 The configuration of the ACV DC-HCB implemented in LVDC study system model 97

6.5 Representation Part A of the Fig 6.3 when a fault is applied 98

6.6 Case I: PSCAD/EMTDC simulation waveforms of the DC-HCB and the DC cable, (a) I_B vs T when DC fault applied at the rectifier side, (b) V_{cp} vs T when DC fault applied at the rectifier side, (c) I_c vs T when DC fault applied at the rectifier side, (d) V_{cs} vs T when DC fault applied at the rectifier side, (e) I_{dc} vs T when DC fault applied at the rectifier side, and (f) V_{dc} vs T when DC fault applied at the rectifier side. 100

6.7 Case II: PSCAD/EMTDC simulation waveforms of the DC-HCB and the DC cable, (a) I_B vs T when DC fault applied at the middle of DC line, (b) V_{cp} vs T when DC fault applied at the middle of DC line, (c) I_c vs T when DC fault applied at the middle of DC line, (d) V_{cs} vs T when DC fault applied at the middle of DC line, (e) I_{dc} vs T when DC fault applied at the middle of DC line, and (f) V_{dc} vs T when DC fault applied at the middle of DC line. 101

6.8 Case III: PSCAD/EMTDC simulation waveforms of the DC-HCB and the DC cable, (a) I_B vs T when DC fault applied closed to the converter, (b) V_{cp} vs T when DC fault applied closed to the converter, (c) I_c vs T when DC fault applied closed to the converter, (d) V_{cs} vs T when DC fault applied closed to the converter, (e) I_{dc} vs T when DC fault applied closed to the converter, and (f) V_{dc} vs T when DC fault applied closed to the converter. 102

List of abbreviations

AC	alternating current
ACV	alternative counter-voltage
CB	circuit breaker
DC	direct current
FCZ	first current zero-crossing
GTO	gate turn-off thyristor
HCB	hybrid circuit breaker
IGBT	insulated-gate bipolar transistor
IGCT	Integrated gate-commutated thyristor
LVDC	low voltage direct current
MCB	mechanical circuit breaker
MOV	metal oxide varistor
SCZ	second current zero-crossing
SSCB	solid-state circuit breaker
TCV	traditional counter-voltage
TIT	total interruption time
TRV	transient recovery voltage

Chapter 1

Introduction

1.1 Problem Statement

The circuit breaker (CB) is an electrical piece of equipment to stop the current flow under abnormal condition and "break" the current path. This is to prevent damage to electrical pieces of equipment and maintain the integrity of the system operation. There are three types of CBs:

1. mechanical circuit breaker (MCB)
2. solid-state circuit breaker (SSCB)
3. hybrid circuit breaker (HCB)

The conventional circuit breaker is a MCB which has a small on-state resistance, and a relatively long interruption time because of the movement of the mechanical parts and the electric arc phenomenon. The SSCB is composed of semiconductor devices. The main advantage of SSCB as compared with the MCB is its short current interruption time, and the disadvantages are the cost and relatively high on-state resistance. Furthermore, due to the voltage and current limitations of semiconductor devices, the SSCB cannot be readily used for large current and high voltage applications. The hybrid circuit breaker is a combination of the MCB and the SSCB. The MCB is used as the main current path which conducts the normal current and the semiconductor switches are used as complimentary switches to assist current interruption. When the metal contacts separate, the current is transferred from the main path (MCB) to the commutation path which includes the semiconductor devices.

Compared to AC, interruption of DC is more challenging. The main reason is the absence of the DC zero-crossings. The main requirements for DC interruption are:

1. The CB has to interrupt within a very short time once the fault current is detected, e.g., between 3-5 ms. Within this time range, the increasing of the current is limited that the normal switches will not be damaged and the internal protection of the converter will not be activated.

2. The over-voltages generated by the CB operation must be low enough to comply with the DC system requirements and the breakdown voltage of the semiconductor devices.

3. The sizes and the costs of the auxiliary elements of the CBs, e.g. capacitors, and inductors have to be limited.

Some manufactures claim that HCB products can interrupt the DC in the range of 5ms, such as ABB S800PV-S. However, these DC-HCBs have neither used widely nor test results provided. As of now, to the best of our knowledge, there is no commercially available DC-CB technology that can meet the above three basic requirements.

1.2 Literature Review

Theoretically, there are two approaches to stop the DC. One approach is to reduce the driving potential to zero and then "break" the current. The second approach is to use a mechanism that acts as a CB and creates an open circuit to interrupt the DC. The latter is the practically viable option.

The first type of MCB for DC was based on the mercury switch [2]. As the switch technology improved, the knife-blade based switches replaced the mercury switches and are still used for low-voltage and low-power applications. The SSCB technology is relatively new and can be used for both the AC and DC interruption. However, it is available for significantly lower current and voltage levels as compared with the MCB. To interrupt the DC, the DC-CB must 1) create a current zero-crossing, and ii) dissipate the energy associated with the system inductances to prevent excessive overvoltages due to the current interruption.

1.2.1 DC Interruption Techniques

The current-zero crossing can be generated by the following methods.

Imposing an oscillatory current component on the DC

To impose an oscillatory current component on the DC which is to be interrupted, a commutation path, which is a passive LC resonance circuit, can be exploited. Fig 1.1 shows a schematic diagram of a passive DC-MCB [3]. When mechanical contacts open in response to a fault identification, a series resonance in the capacitor and the inductor path is established which creates a zero-crossing in the current and enables the MCB to extinguish the arc and open the DC path. The nonlinear metal oxide varistor (MOV) element is to limit the overvoltage due to current interruption and dissipate the associated energy. The DC-MCB can interrupt up the 3kA-DC at voltages up to 5kV in about 13ms [3].

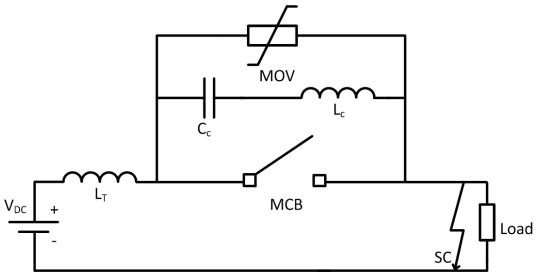

Figure 1.1: A structure of the passive mode DC-MCB

Fig 1.2 shows the circuit diagram of an active DC-HCB [3]. Similar to the passive mode MCB, the DC-HCB also includes a LC resonance circuit. An external voltage source is used to charge the commutation capacitor C_C to a pre-specified voltage level. A SSCB is connected in series with the resonance circuit to prevent the current flow in the LC commutation path before the interruption process starts.

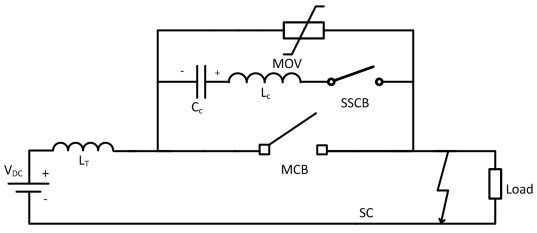

Figure 1.2: A structure of the active mode DC-HCB

Subsequent to a fault current, the SSCB is closed to provide a commutation path and the capacitor imposes a counter-current. The magnitude of the oscillatory current in the commutation path reaches the magnitude of the line current, and the MCB opens at the current zero-crossing . Hence the electric arc in the MCB can be minimized. However, an external voltage source is needed and a high over-voltage may result when the current interruption occurs. Compared to the passive mode MCB of Fig 1.1, the active mode HCB of Fig 1.2 can interrupt the DC faster. The active mode HCB can interrupt up to 5kA DC in less than 1ms at the voltage up to 5kV [3].

Imposing a counter-voltage

The current zero-crossing also can be achieved by generating a counter voltage with the same or larger amplitude than the DC supply voltage V_{DC} by a pre-charged capacitor which is in parallel with the main switch as shown in Fig 1.3 [4].

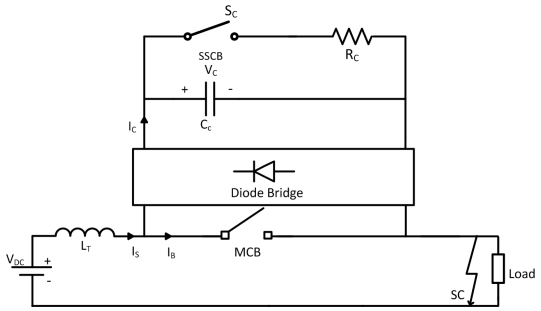

Figure 1.3: A structure of counter-voltage topology DC-HCB

As the fault current is detected, the MCB opens and the line current flows through the commutation path. The energy stored in the system inductor L_T is transferred to the commutation capacitor C_C, and then the energy absorber R_c is inserted to dissipate the energy and maintain the capacitor voltage to its pre-charged voltage level after the fault. The diode bridge is used to enable the bi-directional current flow. Same as the active mode topology of Fig 1.2, an external voltage source and a large capacitor are required for this configuration.

Paralleling a non-linear resistor (MOV)

The third method is to parallel a non-linear resistor with the SSCB. Two different configuration of surge-less DC-SSCB are shown in Fig 1.4 [5].

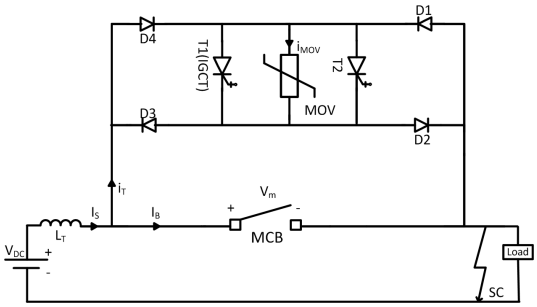

Figure 1.4: (a) A DC-SSCB paralleling a non-linear resistor, and (b) a DC-SSCB with a freewheeling diode

In the system of Fig 1.4(a), a non-linear varistor (MOV) is connected in parallel with a SSCB. When the fault is detected in the load side, the SSCB opens and the load current commutates to the non-linear varistor. Surge voltage across the SSCB is suppressed to the clamping voltage of the non-linear varistor. The clamping voltage should be larger than the DC supply voltage. In this configuration, the interruption time is dependent on the clamping voltage. Smaller clamping voltage results in shorter interruption time, but a larger amount of energy needed to be absorbed by the non-linear varistor. Fig 1.4(b) shows an alternative surge-less DC-SSCB including a freewheeling diode. In this configuration, a non-linear varistor in series with a free-wheeling diode is connected in parallel with the DC source and the SSCB. Under normal conditions, the SSCB remains closed and conducts the load current. Subsequent to a fault, the SSCB opens and the fault current commutates to the free-wheeling diode and the non-linear resistor. In this configuration, since DC source does not supply any power when the SSCB is open, the energy absorbed by the non-linear resistor, during the interruption process, is equal to the energy stored in the overall system inductor L_T, and a relatively small clamping voltage can be chosen. However, to achieve the fast interruption, the energy stored in the system inductor has to be dissipated in a short time. This type of SSCB can interrupt up to 30A DC in 2.5ms under supply voltage of up to 360V[5].

1.2.2 DC-CB Types

Mechanical Circuit Breaker

The MCB can be categorized as oil CB, air CB, vacuum CB and gas CB [6]. The on-state resistance of MCB can be as low as a few $\mu\Omega$ which is much less than that of a SSCB, and its voltage drop under normal condition is less than 100mV. Due to the electric arc

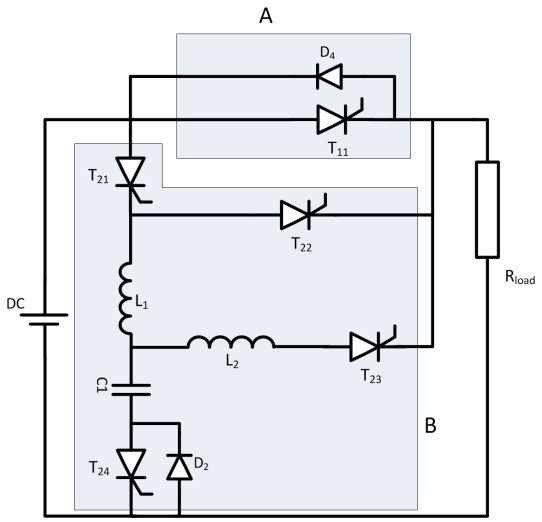

Figure 1.5: Circuit diagram of the DC-SSCB circuit

phenomenon,the MCB interruption time is in the order of several ms. Furthermore, the contact erosion due to the arc necessitates frequent maintenances of the MCB [7] [8].

Solid-state Circuit Breaker

The SSCB is an electrical circuit that includes semiconductor switches, such as the power diode, thyristor, GTO, or IGBT. The on-state resistance of a SSCB is relatively significant and within the range of a few mΩ, and its voltage drop under normal operating conditions is between 1 and 2V [7]. The main issues that have prevented the development of the SSCB are the limitation on maximum fault current carrying capability and blocking voltage of semiconductor switches. With the continuous improvement in semiconductor switches[6], the SSCB is considered to be an economically and technically viable technology for the future grid applications, including medium- and high-voltage DC systems as well. The experiment results of latest development in SSCB technology report 55 A current interruption capability within about 1ms at 120V source voltage[9].

The main advantage of the SSCB as compared with the MCB is the fast and arc-less current flow interruption. The interruption time can be in the range of tens of μs to several ms. Because of the arcless interruption, the life expectancy is significantly higher than that of MCBs. A SSCB which uses thyristors as the main switches is shown in Fig 1.5 [10]. Block A represents the main path and block B represents the commutation path. Since this SSCB is designed to operate under low voltage and low current, it is capable of soft turn-on and fast turn-off.

Hybrid Circuit Breaker

The HCB, conceptually, consists of both mechanical switches and semiconductor switches. A DC HCB with ultra-fast contact opening capability can interrupt up to 1.5 kA DC successfully in less than 1 ms at the voltage of about 4kV[11]. A configuration of a hybrid circuit breaker is shown in Fig 1.6.This HCB uses a non-linear varistor in parallel with the main switch. The diode bridge of this DC-CB enables bi-directional current flow and thus AC applications as well. Under normal conditions, the line current flows through the main path,i.e., MCB, which has a low resistance . Subsequent to a fault, the MCB is activated and also a turn-on signal is issued to the IGCTs. Then, the current is directed to the commutation path. After the line current is fully directed to the commutation path, the IGCTs are turned off. This commutation process generally requires more than 300 μs to make sure that metal contacts of the MCB are sufficiently separated and the arc cannot be reestablished. The energy associated with the opening process is absorbed by the varistor.

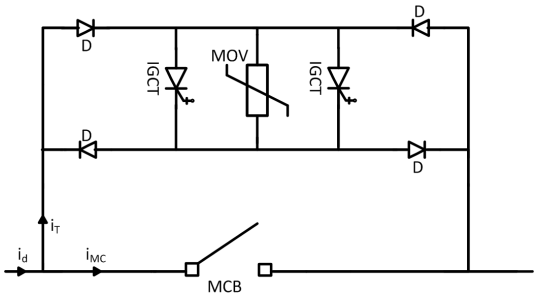

Figure 1.6: Basic configuration of the ultra-fast contact opening HCB

1.3 Thesis Objective

The objective of this thesis is to propose and present feasibility studies of an alternative counter voltage DC-HCB for Low voltage DC (LVDC) distribution system (up to 750V). A structure of proposed alternative counter voltage DC-HCB is shown below in Fig 1.7 as will be described in the subsequent chapters.

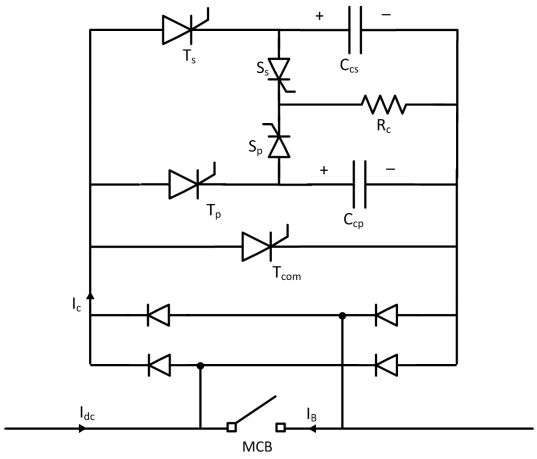

Figure 1.7: A structure of the proposed alternative counter voltage DC-HCB

This DC-HCB can effectively mitigate the arcing process of the MCB thereby reducing contacts erosion. The advantages also include reduced physical size and low blocking voltage of semiconductor devices. The counter voltage DC-HCB based on the widely available components can interrupt the DC up to 5kA under up to 1kV within 5 ms.

1.4 Thesis layout

Fig.1.8 shows the organization of the materials in the thesis. Chapter 2 introduces four potential DC-HCB configurations and their principles of operations. Chapter 2 also describes the low voltage direct current (LVDC) study system and tools adopted in this thesis.

Chapter 3 presents the arc model for time-domain simulation for both the AC and DC interruption. This chapter demonstrates the important of the current zero-crossing for the fault current interruption.

Chapter 4 provides detail analysis and time-domain simulation for the active mode DC-HCB considering the DC arc model from Chapter 3. Chapter 5 provides the feasibility and time-domain simulation studies for two counter-voltage DC-HCBs, i.e, the traditional counter-voltage (TCV) DC-HCB and the proposed alternative counter-voltage (ACV) DC-HCB. The simulation results of both DC-HCB with considering the DC arc model are also presented. From results, one conclude that the proposed ACV DC-HCB is a preferred option to the TCV DC-HCB.

Chapter 6 first compares the proposed ACV DC-HCB with the active mode DC-HCB

and conclude that the performance of proposed DC-HCB is superior to that of the active mode DC-HCB. Then the ACV DC-HCB is proposed to interrupt a 5 kA fault current within 5 ms when the system voltage is up to 1 kV. Finally, the proposed DC-HCB is tested under the LVDC study system to evaluate its performance. Chapter 7 states the conclusion and future work of the thesis.

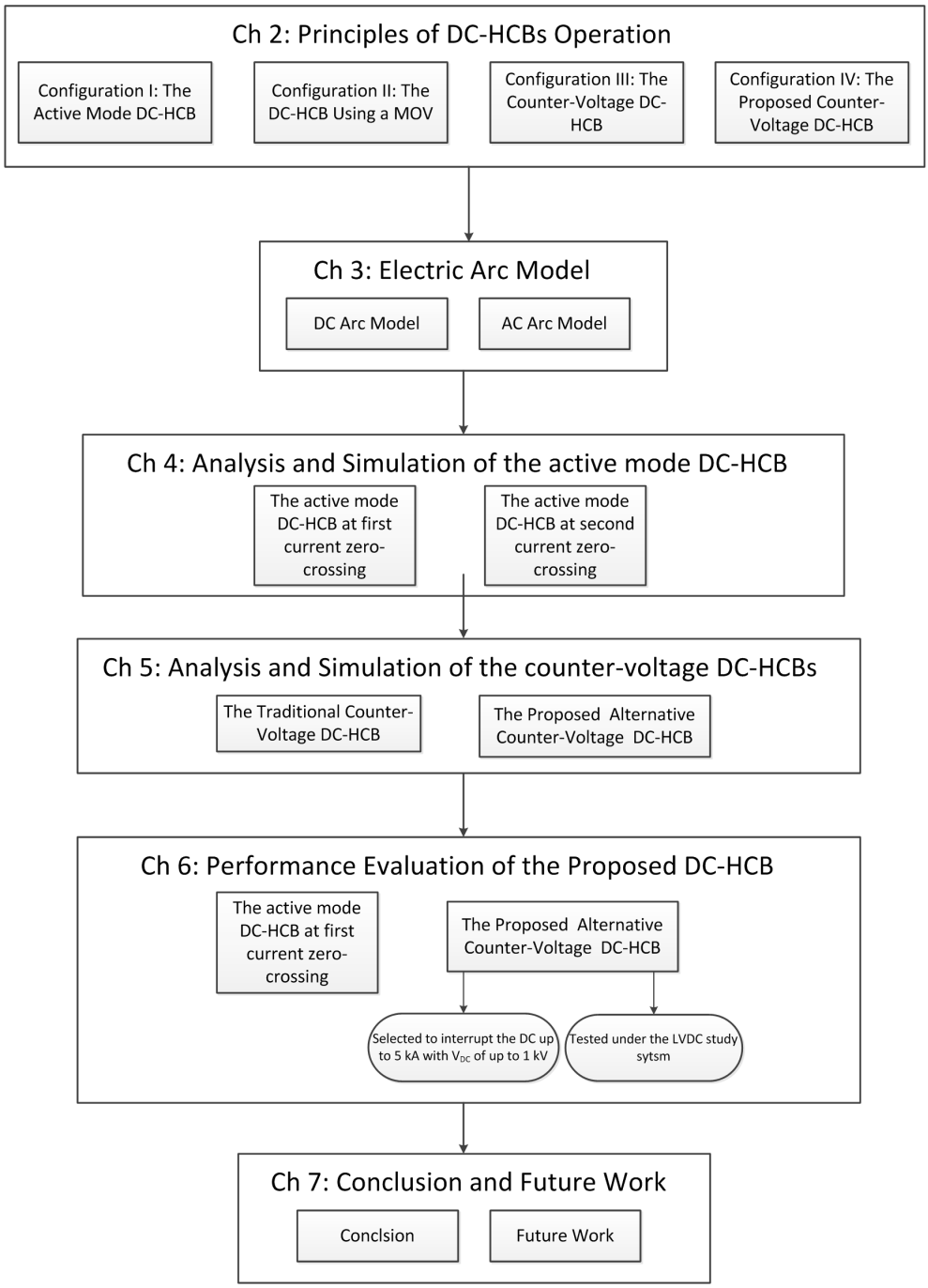

Figure 1.8: Thesis layout

Chapter 2

Principles of Operation of DC-HCBs

2.1 Introduction

In the previous chapter, three different DC interruption techniques were discussed. This chapter discusses a set of DC-CB configurations based on the techniques of Chapter 1 and a new topology is proposed which improves the performance of the DC-CB as compared with the existing configuration. This chapter also introduces a low-voltage (LV) DC system to test the behavior of the proposed DC-CB based on time-domain simulation studies in the PSCAD/EMTDC platform.

2.2 DC-CB Configurations

2.2.1 Configuration I: Active Mode DC-HCB

The active mode topology, Fig 2.1 [12], injects a counter-current to interrupt the DC. This counter-current injection opposes the line current in the main mechanical switch, and imposes current zero-crossings to enable the mechanical switch to clear the arc and interrupt the DC. To achieve this commutation process, an additional circuit which contains a LC resonance circuit and a SSCB (S_C) is required, Fig 2.1. S_C can be either a uni-directional switch or a bi-directional switch. In this configuration, a thyristor is used as a uni-directional semiconductor switch. Two current zero-crossings can be generated, i.e., the first current zero-crossing (FCZ) and the second current zero-crossing (SCZ). The commutation capacitor C_C must be pre-charged and the S_C is used to prevent the current flow before the interruption process starts. The DC zero-crossing can be generated if the

peak magnitude of the counter-current injection exceeds the fault current. Therefore, it is necessary to have prior knowledge of the fault current level. A diode bridge is used to enable bi-directional current flow.

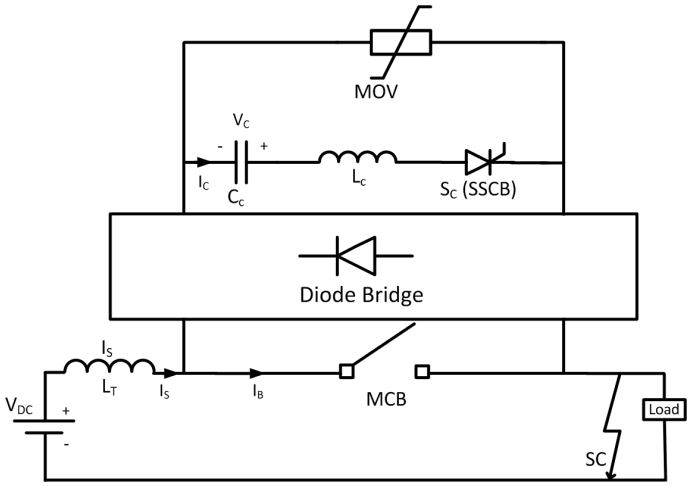

Figure 2.1: A basic configuration of the active mode DC-HCB

Fig.2.2 shows the fault current interruption process, associated with the active mode DC-HCB at the FCZ. Initially, the MCB is closed and the DC flows through the MCB. S_c, Fig 2.1, is open and thus there is no current flows into the commutation path. Subsequent to a fault at t_0, the line current I_S, Fig 2.2(a), increases. A turn-on gating signal is sent to S_C at t_1 when the line current I_S reaches I_{St}. Current oscillations which are generated by the pre-charged commutation capacitor C_C and the commutation inductor L_C oppose the DC flow into the MCB. During this process, both the line current I_S and the commutation current I_C increase. However I_C must increase faster than I_S to produce the current zero-crossing. Hence, a proper combination of L_C and C_C is required to generate at least one current zero-crossing for the MCB. Fig 2.2(b) shows two possible current zero-crossings and the MCB is assumed to open at the FCZ at t_2. Since the operation of the MCB is not instantaneous, the MCB may not be able to fully interrupt the DC at the zero-crossing instant in a real scenario. A current "jump" may happen during the interruption process, so a surge voltage protection is required. In Fig 2.2(c), the interruption process finishes when the line current naturally goes to zero at t_3. C_C is discharged and then charged to the maximum voltage V_f, Fig 2.2(d). If a bi-directional SSCB is used as S_C, multiple current-zeros can be created and the line current oscillates until the line current reduces to zero.

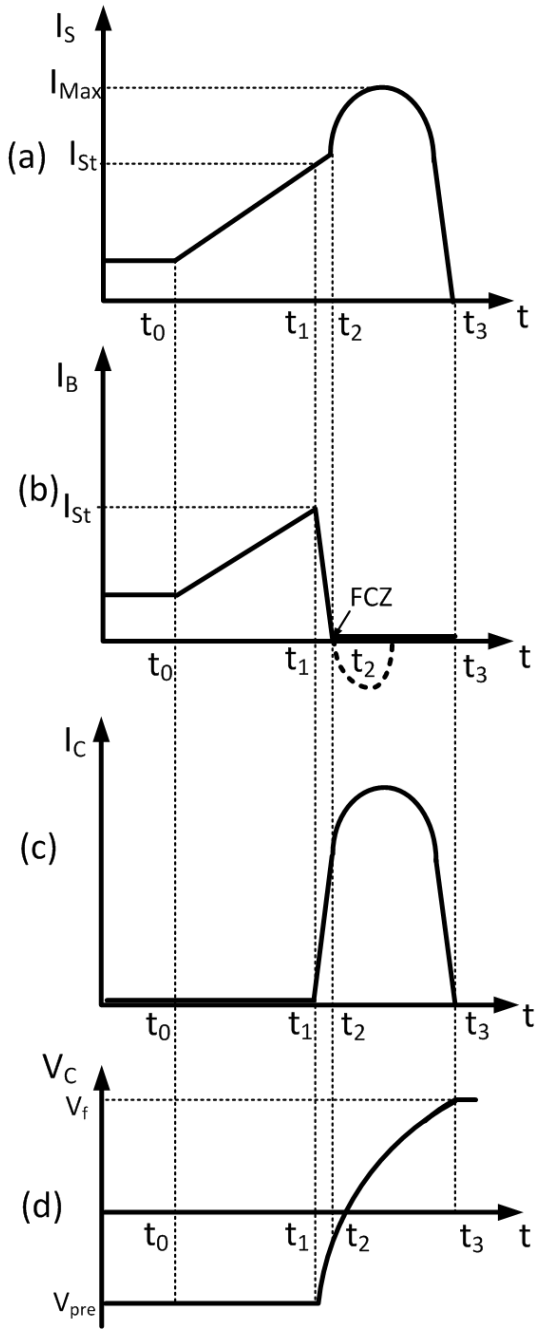

Figure 2.2: Fault current interruption process of Configuration I (FCZ= First Current Zero-crossing), (a) line current I_S, (b) current through the MCB I_B, (c) commutation current path I_c, and (d) voltage of the commutation capacitor V_C.

As a counter-current is introduced by this configuration, the MCB can open at current zero-crossing which effectively extinguished the electric arc. However, the semiconductor devices in the commutation path must withstand the high current and the high blocking voltage.

2.2.2 Configuration II: DC-HCB Based on MOV

The circuit configuration of this DC-HCB uses a metal-oxide varistor (MOV) in parallel with a SSCB (S_C) to achieve DC interruption, Fig.2.3 [11]. In this configuration, S_C must be a fully controllable semiconductor switch, i.e., an IGBT. In the commutation path, the diode bridge enables the bi-directional current flow.

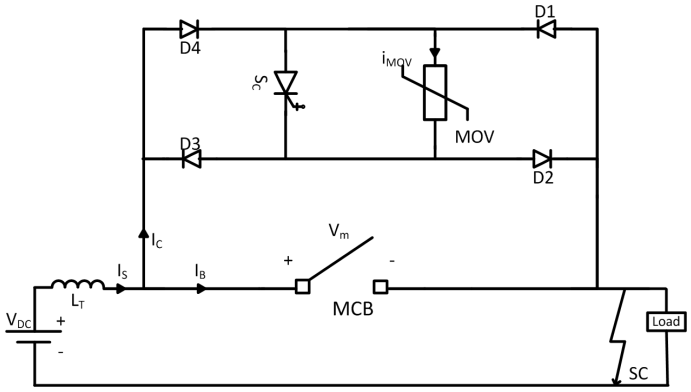

Figure 2.3: A basic configuration of the DC-HCB using a MOV

Fig.2.4 shows the fault current interruption process of the DC-HCB. Before the fault, the MCB is closed and the DC flows through the MCB from the source side to the load side. S_C is open and thus no current flows though the commutation path. Subsequent to a fault at t_1, the line current I_S increases. When I_S, Fig.2.4 (a), reaches the trip level I_{St} at t_2, the fault detecting unit provides an opening command to the MCB and also provides an turn-on gating signal for S_C. A contact separation, at t_2, is followed by an electric arc. The current in the MCB I_B, Fig.2.4 (b), is directed to the power electronic path I_C, Fig.2.4 (c). The commutation time interval (T_{com}), Fig.2.4 (c), finishes at t_3 and the arc is extinguished. The line current I_S, Fig.2.4 (a), flows into the commutation path I_C, Fig.2.4 (c). To prevent re-ignition of the arc, the time interval T_{cond} is required. Once S_c is turned off at t_4, the line current flows into the MOV (I_{MOV}), Fig.2.4 (d). The surge voltage generated by the system inductor increases until it reaches the clamping voltage of the MOV (V_{max}), Fig.2.4 (e), at t_5. The smaller the clamping voltage V_{max}, the larger amount of energy is dissipated by the MOV and the interruption time is longer.

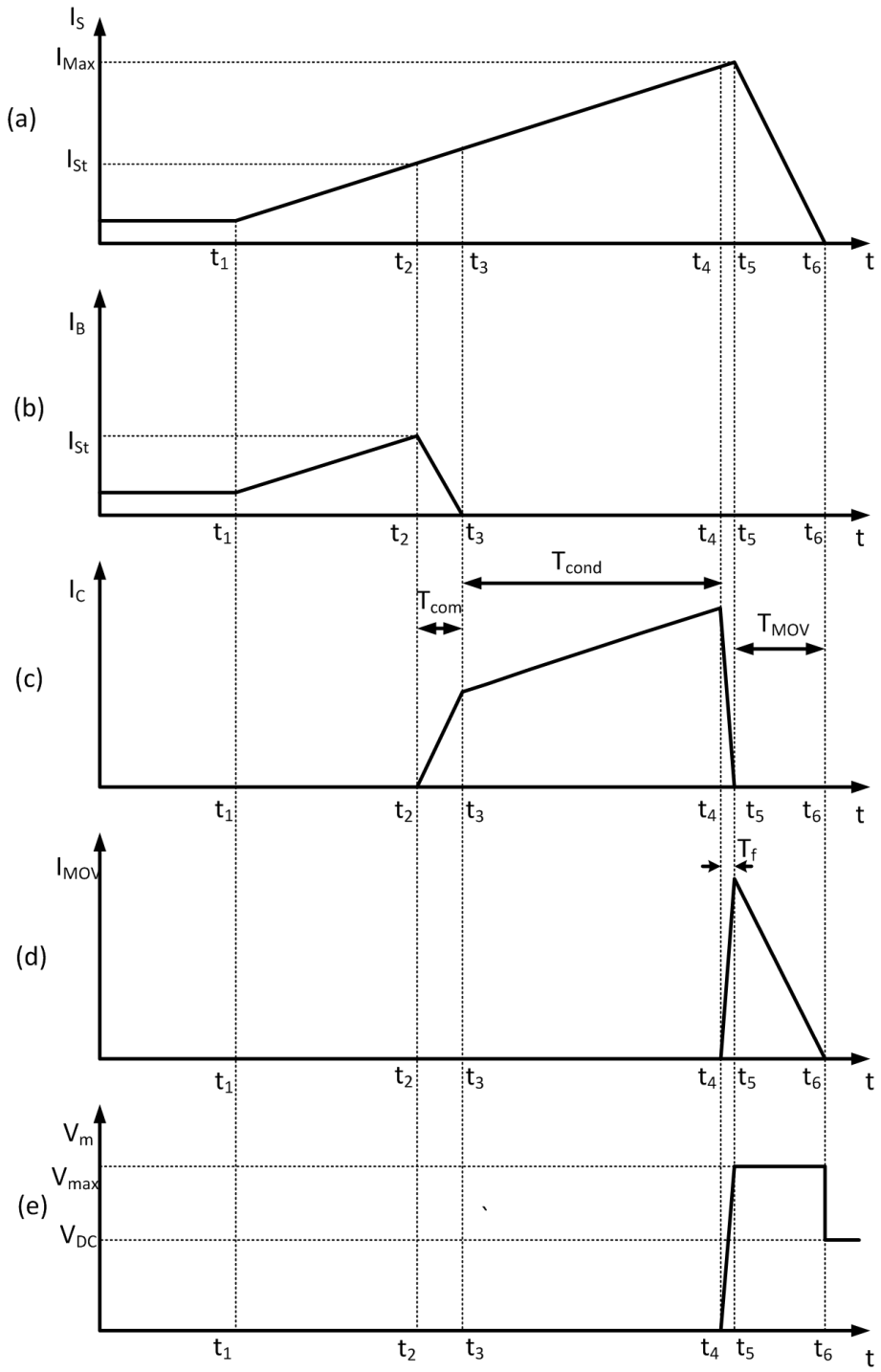

Figure 2.4: Fault current interruption process of Configuration II, (a) line current I_S, (b) current through the MCB I_B (c) commutation current path I_C (d) current through the MOV I_{MOV}, and (e) voltage across the MCB V_m.

The main advantage of this configuration with respect to other configurations is that no capacitors and inductors are used in the commutation path. However, during the

interruption process, the line current increases until the voltage across the MOV reaches its clamping voltage. This requires the semiconductor devices to withstand large current values. Moreover, the possibility of arc re-ignition must be evaluated for this configuration.

2.2.3 Configuration III: Counter-Voltage DC-HCB

The third DC-CB circuit configuration is the counter-voltage DC-HCB as shown in Fig 2.5 [4]. The capacitor C_C is pre-charged to introduce a counter-voltage for interrupting the fault current. The pre-charged voltage of C_C, V_{pre}, must be equal to or larger than the DC supply voltage V_{DC} to effectively reduce the interruption time. Same as the other DC-CBs, the diode bridge is used to enable bi-directional current flow. The fault current interruption process of configuration II is shown in Fig 2.6.

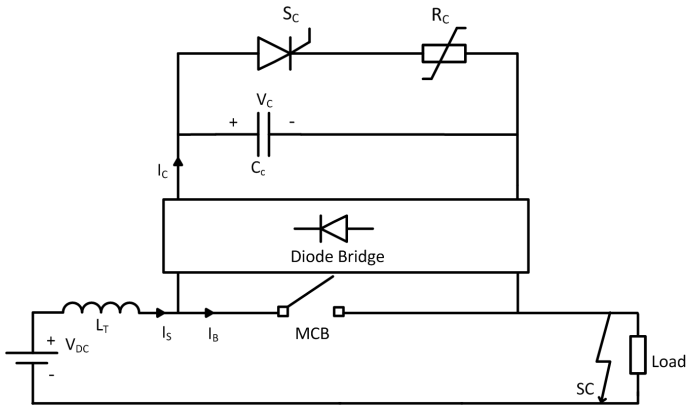

Figure 2.5: A basic configuration of counter-voltage DC-HCB

Subsequent to a fault at t_0, the line current I_S, Fig 2.6 (a), increases. At t_1, I_S reaches I_{St}, Fig 2.6 (a) and the fault detection unit issues an opening signal to the MCB. An electric arc appears across the MCB contacts. The line current I_S starts to commutate from the main path (I_B), Fig 2.6 (b), to the commutation path (I_C), Fig 2.6 (c). This time interval is the commutation time interval T_{com}, Fig 2.6 (b). At the end of the commutation interval t_2, the arc extinguished; the commutation process finishes and the line current (I_S) fully flows into the commutation path (I_C). During the time interval T_{cap}, the commutation current (I_C) decreases, as the voltage of the commutation capacitor, V_C, Fig 2.6 (d), increases. At t_3, The interruption process finishes and V_C reaches the maximum voltage V_f, Fig 2.6 (d). After that, the capacitor is discharged by the resistor R_c by sending a turn-on gating signal to S_C. S_C turns off when V_C reaches to V_{pre} at t_4.

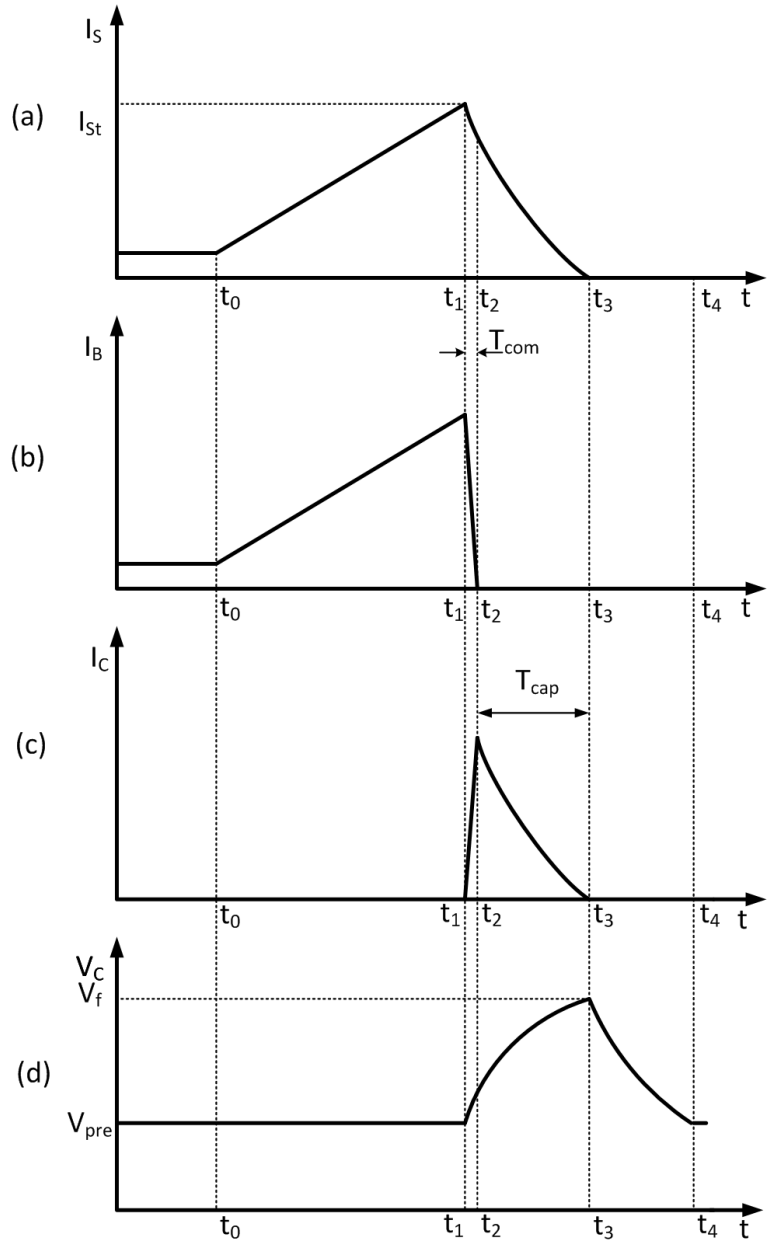

Figure 2.6: Fault current interruption process of Configuration III, (a) line current I_c, (b) current through the MCB I_B, (c) commutation current path I_C, and (d) voltage of the commutation capacitor V_c.

The salient merit of configuration III with respect to other configurations is that it does not require any switching operation during the interruption process. However, it requires a large capacitor for the current interruption.

2.2.4 Configuration IV: Proposed Counter-Voltage DC-HCB

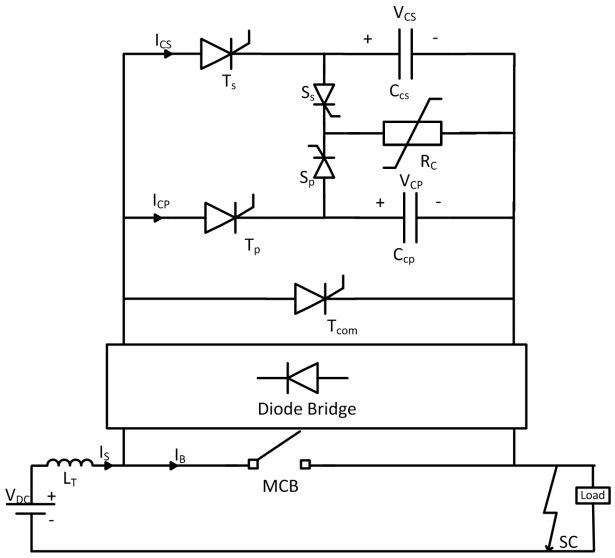

Figure 2.7: A basic structure of proposed counter-voltage DC-HCB

An alternative counter voltage DC-HCB, Fig 2.7, is proposed in this thesis.The proposed configuration is a modified version of the counter-voltage configuration described in [4]. For the traditional counter-voltage DC-HCB, different fault current levels and system inductance values result in different maximum voltage of the commutation capacitor,i.e., V_f. The configuration of Fig 2.7 utilizes two parallel commutation paths, the primary commutation path and the secondary commutation path. Each path includes a SSCB and a pre-charged capacitor. Both capacitors C_{CS} and C_{CP} are pre-charged to the same voltage level V_{pre}. Under normal conditions, the MCB conducts the line current, and the main commutation switch T_{com}, the primary commutation switch T_S and the secondary commutation switch T_P are open. Two other auxiliary switches S_S and S_P also function during the interruption process. Switch T_{com} must be a full-controlled SSCB, i.e, an IGBT. However, the other four switches can be either a full-controlled switches, i.e., IGBTs, or half-controlled switches, i.e., thyristors. In this configuration, T_p and T_s are thyristor. By utilizing two commutation paths, the maximum voltage of each commutation capacitor can be controlled in the proposed DC-HCB. In the traditional counter-voltage DC-HCB, Fig 2.5, a relatively large commutation capacitor C_C, is needed to keep the maximum capacitor voltage to an acceptable level. However, in the configuration of Fig 2.7, a relatively smaller commutation capacitances can be used.

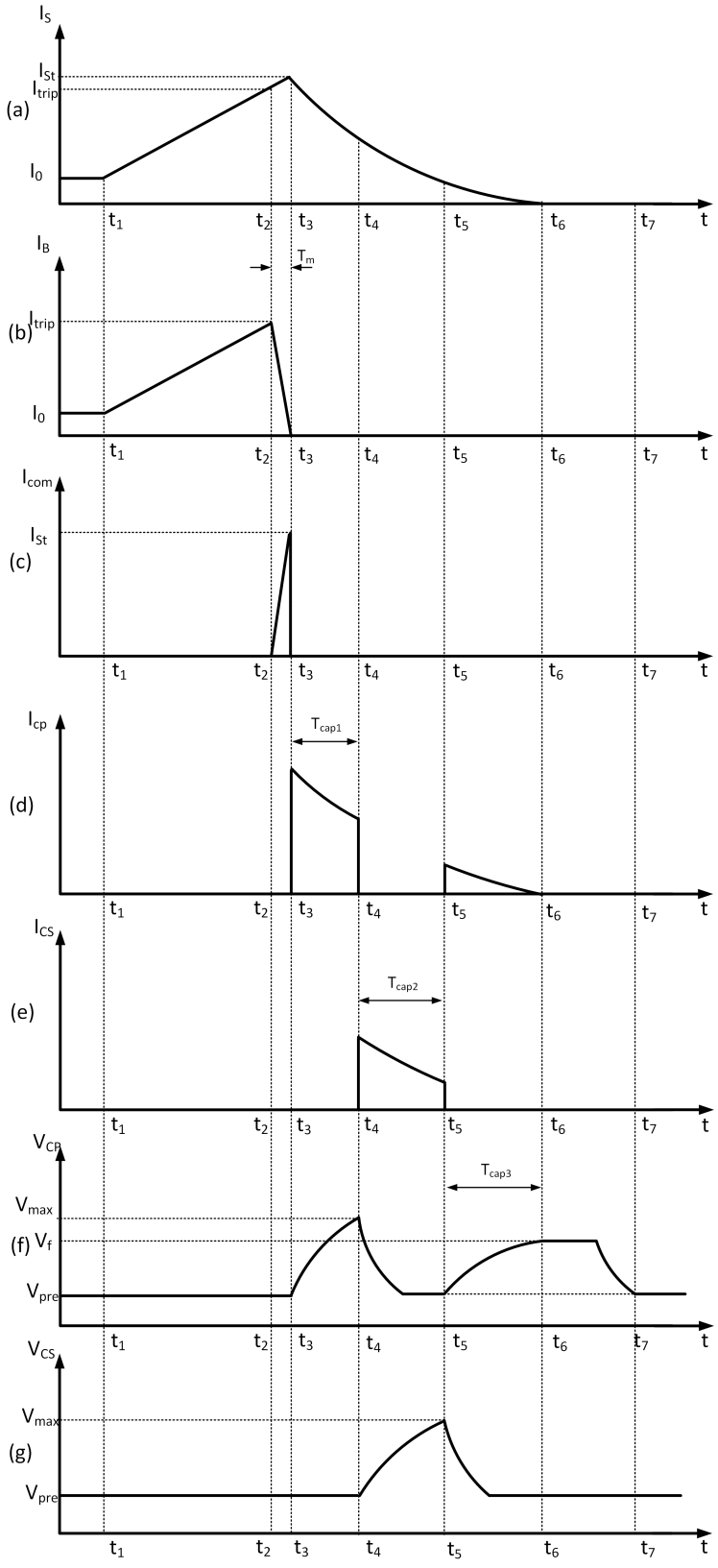

Figure 2.8: Fault current interruption process of Configuration IV, (a) line current I_S, (b) current through the MCB I_C, (c) main commutation current path I_{com}, (d) primary commutation current path I_{CP}, (e) secondary commutation current path I_{CS}, (f) voltage of the primary commutation capacitor V_{CP}, and (g) voltage of the secondary commutation capacitor V_{CS}.

The fault current interruption procedure of the proposed counter-voltage DC-HCB is shown in Fig 2.8. Subsequent to a fault at t_1, the line current I_s, Fig 2.8 (a), increases. An opening signal is sent to the MCB and a turn-on gating signal is also sent to T_{com} at t_2 when the line current I_s reaches the trip current level I_{trip}. The MCB starts to open and the electric arc is generated. At t_3, the current commutation is completed and I_S flows through the main commutation path (I_{com}), Fig 2.8 (c). The commutation time interval is T_m, which is equal to the length of the arcing time. At t_3, I_B reaches to zero, Fig 2.8 (b), accompanied by turning off T_{com} and turning on T_p. During the time interval T_{cap1}, I_S is carried by the primary commutation path (I_{CP}), Fig 2.8 (d). The primary capacitor C_{CP} charges and reaches the maximum voltage V_{max}, Fig 2.8 (f). At t_4, T_S closes. Because the voltage of the primary capacitor V_{CP}, Fig 2.8 (f), is higher than the voltage of the secondary capacitor V_{CS}, Fig 2.8 (g), T_P stops commutation. During the time interval T_{cap2}, I_S is carried by secondary commutation path I_{CS}, Fig 2.8 (e) and C_{CS} charges to V_{max} at t_5, Fig 2.8 (g). Moreover, S_P is closed after t_4 and C_{CP} discharges to pre-charged voltage V_{pre} before the time interval T_{cap2} ends. During the interval T_{cap3}, I_S is carried by the primary commutation path and eventually reduces to zero at t_6. In this time interval, C_{CP} charges to a voltage level lower than V_{max}. S_S is closed after t_5 and C_{CS} discharges to V_{pre} before t_6. In the last time interval, i.e., $t_6 < \mathrm{t} < t_7$, the capacitor C_{cp} discharges to the pre-charge voltage level V_{pre}.

2.3 Comparison of DC-CB Configurations

Configuration I

Configuration I, Fig 2.1, uses a capacitor in series with a inductor, which generates an oscillatory current, to achieve the current zero-crossing. The features of this configuration are: i) only one switch operates during the interruption process, therefore, the switching mechanism is relatively simple, and ii) the MCB opens at the current zero-crossing, thus the electric arc can be effectively reduced. The drawbacks of configurations are: i) the need for an external voltage source to pre-charge the commutation capacitor, ii) the surge voltage generated during the current interruption must be limited, e.g., by an MOV, iii) C_C is a fairly large capacitance, iv) the semiconductor devices must conduct high current I_{max}, Fig 2.2 (a), which is much greater than I_{St}, Fig 2.2 (a), and v) the interruption process may fail if the peak magnitude of the oscillatory current is not able to exceed the line current. Thus the worst-case fault current condition must be identified.

Configuration II

Configuration II uses a MOV in parallel with a full controllable semiconductor switch, Fig 2.3. The merits of this configuration are: i) no external voltage source is needed, and ii) no commutation capacitors and inductors are used. The disadvantages of configurations are: i) the semiconductor devices must conduct large current I_{MAX}, Fig.2.4, ii) the activation time of the MOV is long compared to the turn-on delay of the SSCBs, and iii) the re-ignition of the electric arc must be considered.

Configuration III

Configuration III, Fig 2.5, is based on the counter-voltage approach, and uses a charged capacitor during the interruption. The merits of Configuration III are: i) the interruption mechanism of counter-voltage topology is the simplest as compared to other topologies and does not require switching operations, and ii) the semiconductor devices need to conduct relatively low current, which is equal to the trip level current I_{St}, Fig 2.6 (a). The drawbacks of Configuration III are: i) a large C_C is needed to reduce the blocking voltage of the semiconductor devices, and ii) with different fault current levels and system inductances, the maximum capacitor voltage V_f , Fig 2.6 (d), varies.

Configuration IV

Compared to other topologies, Configuration IV, Fig 2.7, requires multiple commutation paths to carry out the current interruption. The disadvantage of this Configuration is: the switching mechanism to enable the current commutation required five semiconductor switches. In spite of multiple commutation paths, the configuration provides the following advantages: i) small capacitors can be used in the commutation path, thus reduced the weight and the size, ii) the semiconductor switches do not need to withstand large blocking voltage, iii) the semiconductor switches conduct a relatively low current, I_{max}, Fig 2.8 (a).

In the following chapters, the performance of Configuration I and Configuration III are simulated in time-domain in detail and compared with the proposed counter-voltage configuration (Configuration IV). The DC-HCB using the MOV (Configuration II) is not considered any further. The reason is that the activation time of the MOV is long compared to the turn-on delay of the SSCBs. Hence, the MOV is a better choice as a secondary protection device than the primary protection CB.

2.4 Study System

The DC study system is based on the Low voltage direct current (LVDC) distribution system [13]. A structure of the LVDC distribution network is shown in Fig 2.9. The LCC operates as a rectifier, Part A of Fig 2.9, and controls the DC line current to its reference value. The VSC operates as an inverter, Part B of Fig 2.9, and controls the DC line voltage to its reference value. The LVDC study system is introduced to test the behavior of the proposed counter-voltage DC-HCB, and the proposed DC-HCB is located close to the VSC.

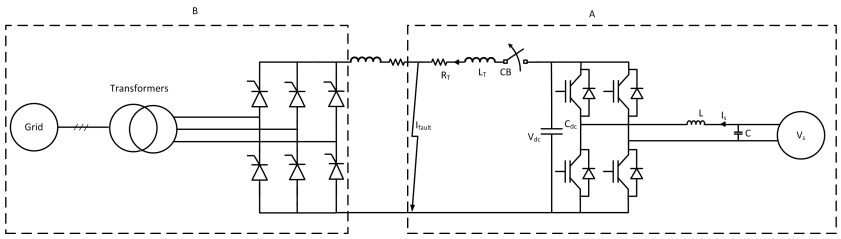

Figure 2.9: The structure of the LVDC distribution network

Parameters of a typical DC power cable is shown in Table 2.1, where L_c is DC cable inductance per kilometer and R_c is DC cable resistance per kilometer. It is considered that the maximum cable length in the steady system is 2 km. Therefore, when the fault is applied to different locations of the DC line, the effective DC inductance L_T, Fig 2.9, and the effective DC resistance R_c, Fig 2.9, vary within their maximum values of 500 μH and 0.2 Ω respectively.

Table 2.1: Parameters of a typical DC cable

Parameters	Value
L_c	250 μH/km
R_c	0.1 Ω/km

2.5 Methodology

This thesis focuses on the feasibility and simulation study of DC-HCBs, i.e., the active mode DC-HCB and the counter-voltage DC-HCB. For each of the DC-HCBs, the analysis of the interruption stages with the associated model of the DC-HCB are presented. Then,

the dynamic performance of the each DC-HCB is demonstrated based on the MATLAB platform. Both of these steps do not consider the DC arc model. Finally, the simulation studies are conducted based on using the PSCAD/EMTDC platform including the DC arc model.

2.6 Conclusion

This chapter discussed four potential DC-HCBs, i.e., active mode DC-HCB (Configuration I), DC-HCB based on MOV (Configuration II), counter-voltage DC-HCB (Configuration III) and proposed counter-voltage DC-HCB (Configuration IV). The principles of operations of each DC-HCB were presented, and the merits and drawbacks of each DC-HCB were also discussed. The DC-HCB based on MOV will not be considered any further, because the activation time of the MOV is longer than the turn-on delay of the SSCBs. Therefore, Configuration I, Configuration III are compared with Configuration IV in the following chapters. This chapter also introduced the LVDC study system for performance evaluation of the proposed DC-HCB. Finally, we introduced that MATALB and PSCAD/EMTDC are the tools adopted for our thesis studies.

Chapter 3

Electric Arc Model

3.1 Introduction

The arc model is a mathematical description of the electrical characteristics of the arc. The arc models have been originally developed for understanding of the current interruption process for the MCB [14]. The physical phenomena of the arc during the current interrupting is complex and generally even the non-linear models do not fully represent the complex physical processes inside the circuit breaker, but to a large extend can describe the electrical behavior of the circuit breaker in the context of the overall system behavior. Due to the complexity of the electric arc, a single arc model does not represent the arc behaviour in all voltage ranges and operating conditions.

In the previous chapter, for the different DC-CB topologies, the arcing time can be effectively reduced when the MCB is used as the main switch. As a result, the arc model for the DC system is a requirement for the DC interruption. This chapter first introduces the fundamental of electric arc, and then investigates the arc model for both AC and DC conditions. Both AC arc model and DC arc model are simulated in the PSCAD/EMTDC platform. The reason for introducing the AC and the DC arc models is to highlight the differences. The developed DC arc model will be used in the subsequent chapters for the overall DC-CB behaviour evaluation.

3.2 Arc Phenomenon Under AC and DC

This section firstly introduces the fundamentals of the electric arc, and then investigates the behavior of the electric arc under DC and AC. The objectives of this section are to show the differences between interruption process of the DC and that of the AC, and adopt the induced DC arc model in the subsequent chapters.

3.2.1 Electric Arc Fundamentals

Electrical arc is a self-sustained electrical discharge phenomenon that has a low voltage drop. It can sustain a large current and behaves "largely" similar to a non-linear resistance whose dissipated power can be as large as 10,000 kW[2]. A general voltage-current (VI) characteristic of the electrical arc is shown in Figure 3.1.

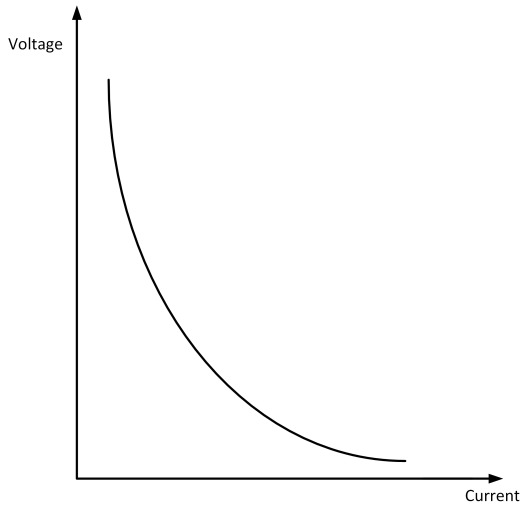

Figure 3.1: Voltage-current characteristic of an electric arc

Generally, electrical arc requires just a low voltage to sustain itself. For example, to sustain electrical arc in the air, only 15V is needed. When the voltage across the contacts at both side of the arc is around 10 kV and the current through the contacts is about 5A, the electric arc length can be as long as 7 m in the air [2]. Therefore, it is not realistic to extinguish the electric arc just by increasing the length of electric arc, i.e., distance between CB contacts, under all conditions.

The arc can be categorized as low pressure arc and high pressure arc, in a vacuum environment and in a variety of gases. A high pressure arc exists at or above atmospheric

pressure. A low pressure arc presents below atmospheric pressure or in a vacuum environment and similarly exhibits some of the basic characteristics of the high pressure electric arc. Figure 3.2 shows the typical voltage distribution of the high pressure arc.

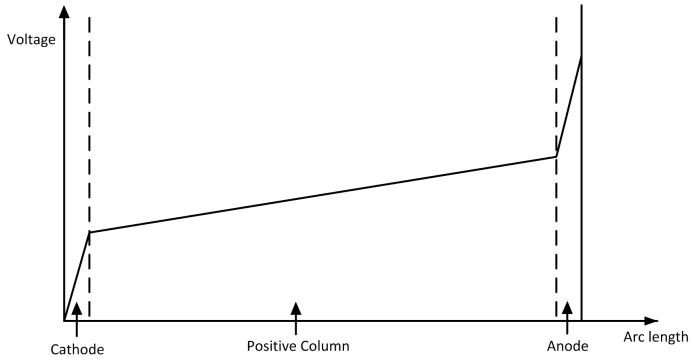

Figure 3.2: Voltage distribution of high pressure arc column

There are three columns in the arc of Fig 3.2, the anode, the positive column and the cathode. The horizon axis of Fig 3.2 shows the relative length of each column, and the vertical axis demonstrates the voltage drop of each column. The lengths of the anode and cathode are relatively short, and the voltage drop of each column is relatively large. In contrast, the positive column is relatively long and exhibits low voltage drop. The high pressure arc appears as a bright column, characterized by a small, highly visible burning core. The temperature is the highest in the middle of arc which can reach 4000 K or higher [2]. The electric arc has large amount of energy stored inside and causes strong erosion to the contacts at its both ends. extinction of the electric arc is the indication that the circuit is disconnected through the arc path and the current flow has stopped.

3.2.2 Interruption of AC

In an AC circuit, the current zero-crossings can be achieved naturally. This is because, in an AC, the instantaneous value of the current passes through zero twice each cycle. Therefore, to interrupt an AC, it is only necessary to prevent the re-ignition of the arc once the current reaches zero. As a result, the de-ionization of the arc gap close to the time of a natural current zero is important. Successful current interruption depends on if the "dielectric strength" of arc gap is greater than the transient recovery voltage (TRV), that is forced across the arc gap in attempt to re-establish the flow of the current. The dielectric strength of the arc gap mainly depends on the interrupting devices, while the TRV across the arc gap depends on the overall circuit parameters. Fig 3.3 shows two

cases corresponding to the AC current interruption. u_d represents the dielectric strength of arc and u_{rr} stands for TRV of the system. Fig 3.3(a) shows the dielectric strength is not enough, and then re-ignition happens. In contrast, in Fig 3.3(b), the recovery voltage is not able to establish the current flow and then the current is interrupted.

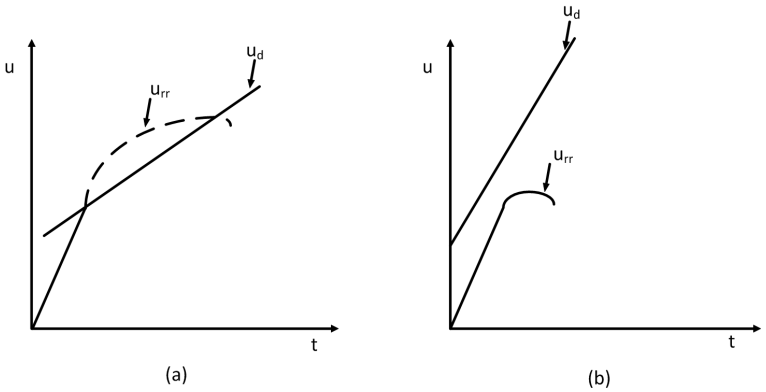

Figure 3.3: Two cases of AC interruption

For the AC, the degree of success to interrupt the current is largely influenced by the system parameters. When a system is dominantly resistive, the abrupt current interruption is practically possible. If the system is mainly inductive, a sudden change of the current may results in a surge voltage across the system inductor. As a result, the TRV could be significant and the interruption process may fail.

3.2.3 Interruption of DC

The absence of the DC zero-crossings must be overcome and the main function of DC-CB is to create current zero-crossings. In general, two methods can be used to create a current zero-crossing. In the first method, the current zero-crossing imposition is done by increasing the arc voltage V_{arc} to a level that is equal to, or higher than the system voltage V_{DC}, Fig 3.4 , as will be discussed in the following paragraphs. Another method to interrupt the DC is based on the current commutation. The commutation process generally needs additional circuit in parallel with the main CB. The concept of commutation was described in Chapter One and Chapter Two.

Generally, the result of increasing the arc length is an increase in the arc resistance. In Case A, Fig 3.4 (a), a DC circuit contains a uni-directional voltage source V_{DC}, which is in series with resistance R and the MCB. When the CB opens, an electric arc is generated and the arc voltage V_{arc} is the $V_{DC} - Ri$. As the arc length increases, the arc resistance

R_{arc} increases and the voltage across R drops. The arc voltage increases until it is equal to the system voltage. Then the arc is extinguished. In Case B, Fig 3.4 (b), the DC circuit contains the voltage source, the system inductor L, the system resistor R and the MCB. When the MCB opens, the electric arc is generated across the contacts and the arc voltage V_{arc} of the inductive circuit is expressed as,

$$V_{arc} = (V_{DC} - Ri) - L\frac{di}{dt}. \tag{3.1}$$

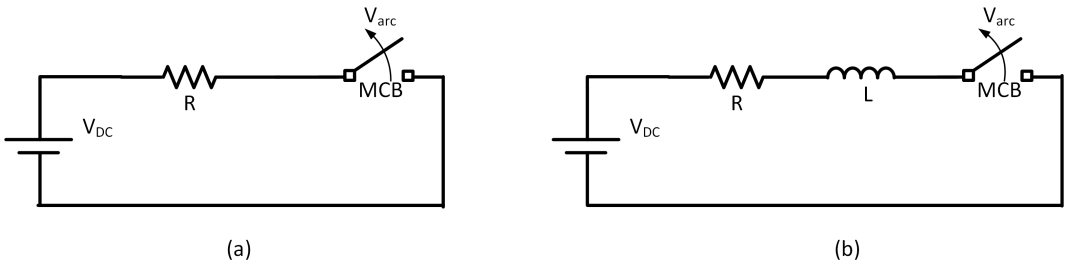

Figure 3.4: Two cases of DC system, (a) Case A: DC circuit without a system inductor, and (b) Case B: DC circuit with a system inductor

A sudden change of the current i results in a large surge voltage across the inductor. In order to extinguish the arc, the arc voltage must equal to this surge voltage which requires a large "dielectric strength" in the gap. Moreover, it extends the time duration of the arc and strong erosion of the contacts. Therefore, increasing the arc length when interrupting DC in the presence of series inductance is not the preferred practicable approach.

3.3 Arc Models

Previous section discusses the operation of the MCB during the electric arc. The main requirements of the AC interruption include (i) opening the CB at the first current zero-crossing and (ii) preventing re-ignition of the arc when the CB opens. The main objective of developing an AC arc model is to quantitatively describe the relationship between these characteristics. Then we describe the DC arc model, and by implementing the DC arc model in the PSCAD/EMTDC, and investigate the DC arc behaviours without the commutation path. This study highlights the importance of the commutation circuit for DC interruption. The DC arc model will be used in the following chapters for performance evaluation of the DC-CBs.

3.3.1 AC Arc Model

This section mainly introduces two arc models, Mayr arc model and Cassie arc model to investigate the different arc behaviours when the CB opens at different current levels. Mayr arc equation is an approximation of the electric arc behavior in the low current range, i.e., in the vicinity of the current zero-crossing. In contract, Cassie arc equation represents an approximation for high current electric arc, i.e., at the maximum (peak) current [15]. Based on these two AC arc models, two simulation studies are carried out in the PSCAD/EMTDC. One study simulates the case when the MCB opens at the instant of current zero-crossing and the other investigates the arc behaviours when the MCB opens at the instant of the maximum (peak) current. The propose of these two studies is to emphasize the importance of opening the CB at the first current zero-crossing and preventing re-ignition of the electric arc.

The key feature of arc model is to use non-linear arc conductance or arc resistance to represent the arc dynamic behavior. Generally, the AC arc model is a set of (one or two) ordinary differential equations that relates the arc conductance to the power supplied to the plasma channel, power transported by cooling and radiation.

In the early 1900s, A.M Cassie and O. Mayr conducted tests to empirically represent the electric arc [15]. Even as of now, two of the most well known and widely used AC arc models are the "Mayr arc equation" and the "Cassie arc equation". Mayr arc equation is a mathematical description of the electric arc behaviour at the low current level, as described by

$$\frac{1}{g_m} = \int \frac{1}{\tau}(\frac{u_{arc} i_{arc}}{P_0} - 1)dt, \tag{3.2}$$

where u_{arc} and i_{arc} are the instantaneous values of arc voltage and current, g_m is the dynamic conductance of electric arc by the Mayr equations, τ stands for the time constant of the electric arc, and P_0 represents the dissipated power, considered as a constant. Cassie arc equation is applied for representation of the high current electric arc behaviours

$$\frac{1}{g_c} = \int \frac{1}{\tau}(\frac{u_{arc}^2}{u_0^2} - 1)dt, \tag{3.3}$$

where τ represents the time constant of the electric arc at the high current level, and u_0 is a constant which stands for the initial value of the electric arc voltage.

There are other AC arc models , e.g., Schwartz and Schavemaker models which are

derived from the Mayr and Cassie arc equations. For example, Schwartz arc model, (3.4), introduces parameters α and β which are the exponential parameters of the electric arc conductance, i.e.,

$$\frac{1}{g_m} = \int \frac{1}{\tau g^{\alpha}} (\frac{u_{arc} i_{arc}}{P_0 g^{\beta}} - 1) dt. \tag{3.4}$$

The Schavemaker arc model, described in (3.5), (3.6) and (3.7), considers the electric arc conductance (g_t) as the series combination of the Mayr arc conductance (g_m) and Cassie arc conductance (g_c) and provides a representation of the arc in a wider voltage range,

$$\frac{1}{g_m} = \int \frac{1}{\tau_m} (\frac{u_{arc} i_{arc}}{P_0} \frac{g_t}{g_m} - 1) dt, \tag{3.5}$$

$$\frac{1}{g_c} = \int \frac{1}{\tau_c} (\frac{u_{arc}^2}{u_0^2} \frac{g_t}{g_c} - 1) dt, \tag{3.6}$$

$$\frac{1}{g_t} = \frac{1}{g_c} + \frac{1}{g_m}. \tag{3.7}$$

Since most of the AC arc models are based on the Mayr and Cassie arc models [15], we choose the Mayr and the Cassie arc equations to simulate two cases of arc behaviour when the CB opens at the instant of current zero-crossing and in the vicinity of the maximum current. The objective of the simulations is to emphasise the importance of the current zero-crossing in an AC circuit.

For our simulation studies, the parameters for the Mayr arc model and the Cassie arc model are obtained from [16] as shown in Table 3.1. The study system is shown in Fig 3.5, [16], and represents a highly inductive circuit.

Table 3.1: Parameter values for Mayr and Cassie arc models

Arc model	Parameter values
Mayr	$P_0 = 3.09 * 10^4 W, \tau_m = 0.3 \mu s, g_0 = 10^4 s$
Cassie	$u_0 = 3850 V, \tau = 1.2 \mu s, g_0 = 10^4 s$

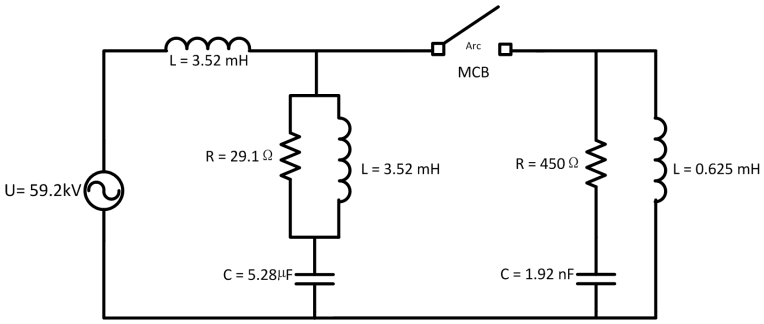

Figure 3.5: Study system for the AC arc model

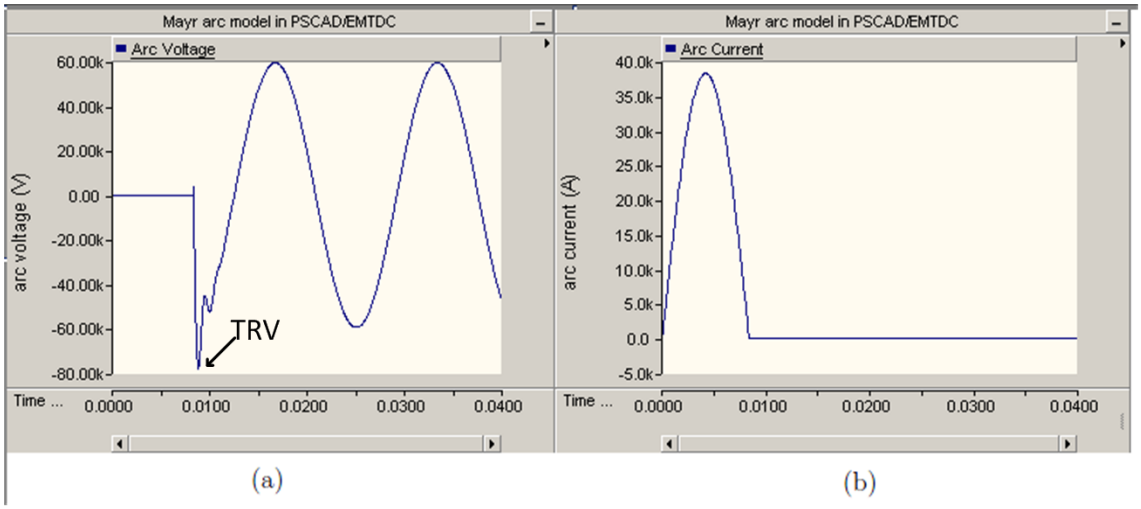

Figure 3.6: Behavior of the Mayr arc model when CB opens at the current zero-crossing instant, (a) arc voltage of Mayr arc model (Case A), and (b) arc current of Mayr arc model (Case A).

Fig 3.6 shows the behavior of the Mayr arc model when the MCB opens at the current zero-crossing instant. Fig 3.7 shows the behavior of the Cassie arc model which the MCB opens in the vicinity of its maximum (peak) current. Since the study system is highly inductive and there is no commutation path to prevent the re-ignition of the electric arc, the transient recovery voltage (TRV) builds across the CB because of the over-voltage generated by the system inductance.The TRV, in Case A, Fig 3.6, is approximately 1.3 time large than the System voltage. In case B, Fig 3.7, the MCB opens at the instant of the maximum current. The current is interrupted in about 50 μs and the TRV builds up to about 10 times of the system voltage. This investigation concludes that interruption of non-zero current, without the use of an auxiliary path, results in extremely high voltage voltages which requires high dielectric strength of the arc medium to withstand the voltage. This translates into higher cost and volume. When the dielectric strength

of the CB gap is not adequate, the re-ignition of the electric arc occurs and the current interruption process fails. Higher TRV requires stronger dielectric strength of the gap medium.

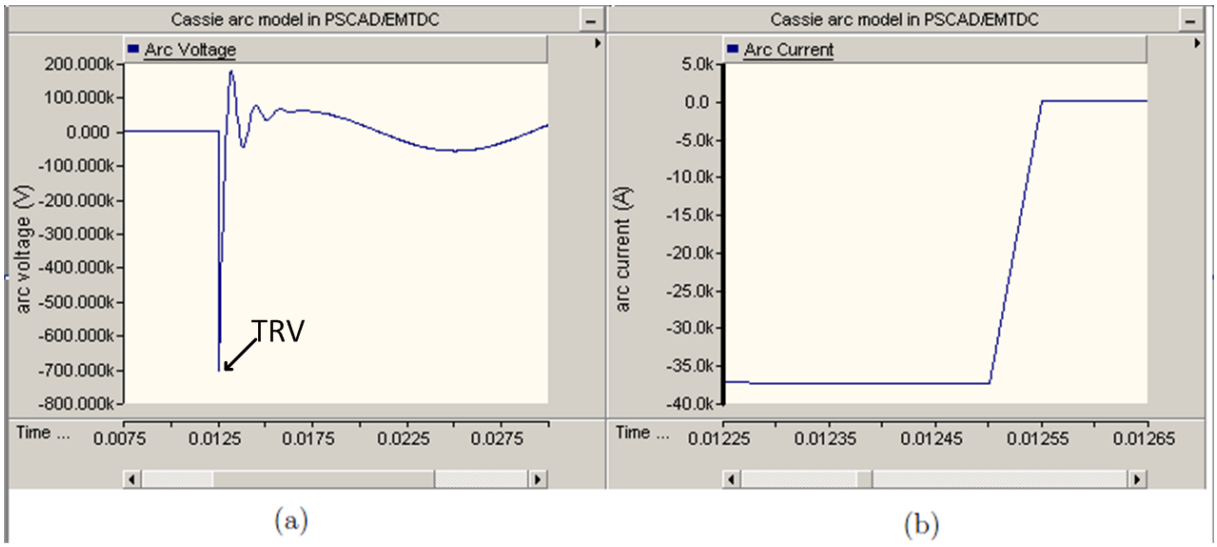

Figure 3.7: Behavior of the Mayr arc model when CB opens at the maximum (peak) current, (a) arc voltage of Cassie arc model (Case B), and (b) arc current of Cassie arc model (Case B).

3.3.2 DC Arc Model

In contrast to the AC arc, the DC arc behaviour has neither been extensively investigated nor its model widely developed/appiled. This section introduces the DC arc model by Paukert [17], to investigate the DC arc behaviors without the commutation path. The objective of this study is to quantitatively emphasizes the importance of the commutation path for DC interruption. In the following chapter, the DC arc model will be implemented into the DC-HCB models to evaluate the performance of the active mode and counter-voltage DC-HCBs.

The Ayrton DC arc model, developed in 1902, represents the DC "steady-state" arc behavior for a small gap (few mm) [18] by

$$V_{arc} = A + BL + \frac{C + DL}{I_{arc}}, \tag{3.8}$$

where V_{arc} and I_{arc} represent the instantaneous values of arc voltage and arc current, A stands for the electrode voltage drop, B represents the voltage gradient of the electric arc,

and C and D describe the nonlinear characteristic of the arc, and L is the arc length. The Ayrton model is developed for carbon electrodes. In the 1920s, Nottingham proposed a DC arc model for several electrode material [19], i.e.,

$$V_{arc} = A + \frac{B}{I_{arc}^{n}}. \tag{3.9}$$

The Nottingham equation is applicable to the DC arc length of 1.0 to 10.0 mm. In (3.9), A and B are dependent on both the arc length and the electrode material, and n is only dependent on the electrode material, and is smaller than 1.

In 1991, Stokes and Oppenlander performed exhaustive studies of free-burning arc in the open air [20], and introduced the concept of transit point, as shown in Fig 3.8. The arc behavior is different when the current through the gap medium is below or above the transit point. When the arc current is below the transit point, the arc has the negative V-I characteristics which indicates that the slopes of V and I are negative. However, the arc exhibits a positive V-I characteristics which means that the slopes of V and I are positive, when the current is higher than the transit point current. The transit point current varies based on the length of the electrode gap as described by,

$$I_t = 10 + 0.2 z_g, \tag{3.10}$$

where z_g represents the length of electrode gap. Stokes and Oppenlander also developed an expression for the arc resistance R_{arc} above the transit current by

$$R_{arc} = \frac{20 + 0.534 z_g}{I_{arc}^{0.88}}. \tag{3.11}$$

In 1993, Paukert published a set of AC and DC empirical arc models [17]. The applicable currents are in the range of 0.3A to 100kA and the electrode gaps from 1 to 200 mm. Furthermore, the transit current is set to be 100A for all DC cases. Table 3.2 and Table 3.3 list a set of Paukert's empirical arc voltages and arc resistances under different electrode gap lengths.

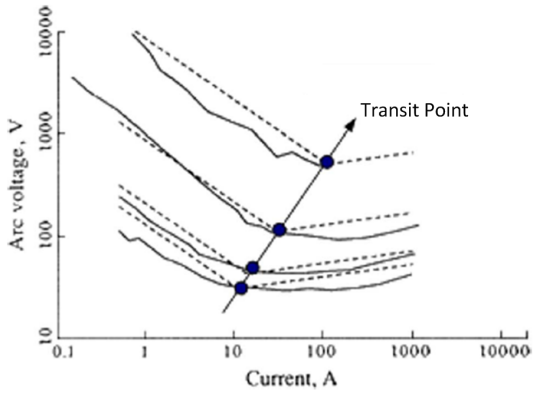

Figure 3.8: V-I characteristic for vertical arcs burning against aluminium electrodes (Stokes and Oppenlander) [1]

Table 3.2: Paukert's empirical arc voltages

Electrode Gap(mm)	Arc voltage(I≤100A)	Arc voltage(100A≤I≤100kA)
1	$36.32I_{arc}^{-0.124}$	$13.04I_{arc}^{0.098}$
10	$105.25I_{arc}^{-0.239}$	$16.68I_{arc}^{0.163}$
50	$262.02I_{arc}^{-0.310}$	$28.35I_{arc}^{0.190}$
100	$481.20I_{arc}^{-0.350}$	$34.18I_{arc}^{0.194}$
200	$661.34I_{arc}^{-0.383}$	$52.63I_{arc}^{0.264}$

Table 3.3: Paukert's empirical arc resistances

Electrode Gap(mm)	Arc resistance(I≤100A)	Arc resistance(100A≤I≤100kA)
1	$36.32I_{arc}^{-1.124}$	$13.04I_{arc}^{-0.902}$
10	$105.25I_{arc}^{-1.239}$	$16.68I_{arc}^{-0.837}$
50	$262.02I_{arc}^{-1.310}$	$28.35I_{arc}^{-0.806}$
100	$481.20I_{arc}^{-1.350}$	$34.18I_{arc}^{-0.759}$
200	$661.34I_{arc}^{-1.283}$	$52.63I_{arc}^{-0.736}$

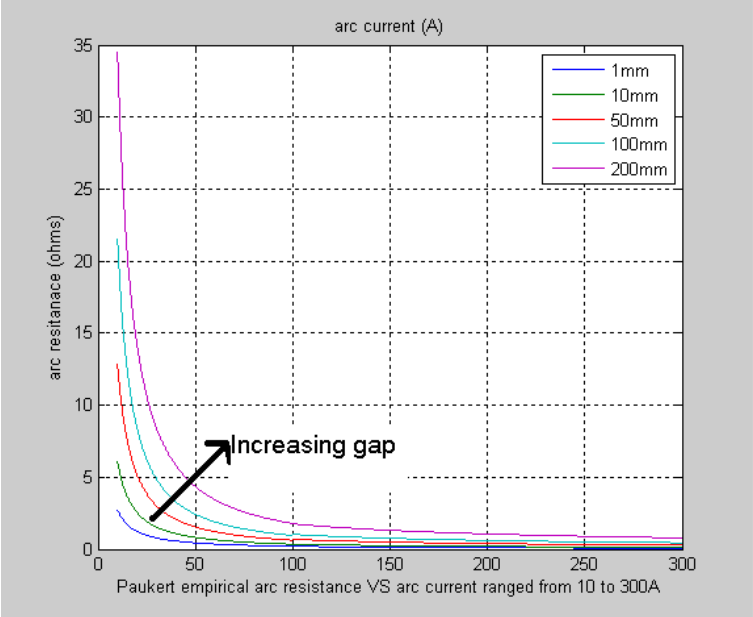

Figure 3.9: Paukert's empirical arc resistance versus arc current ranged from 10 to 300A with different length of electrode gap

The DC arc models share the following common characteristics :
i The arc resistance is a non-linear function of the gap length, the electrode material and the arc current.
ii If the DC is below (above) the transit point current , the DC electric arc has a negative (positive) V-I characteristic.

Fig 3.9 graphically shows the arc current versus the arc resistance of Paukert's empirical arc model, Table 3.3. Fig 3.9 demonstrates that:
• The arc resistance increases as the contact gap length of the CB increases.
• With increasing arc current, the arc resistance decreases. The arc resistance changes rapidly at the low current levels and approaches a relatively constant value at high current levels.
• The arc can be easily maintained in the open air. The arc resistance is small when the electrode gap length is between 1mm to 200mm.

Based on Table 3.3,

• When the DC level is below the transit point current ($I_{arc} \leq 100$A):

$$R_{arc,b} = K_a I_{arc}^{-P_a}, (P_a > 1). \tag{3.12}$$

• When the DC level is above the transit point current($I_{arc} > 100$A):

$$R_{arc,a} = K_b I_{arc}^{-P_b}, (0 < P_b < 1). \tag{3.13}$$

In (3.12) and (3.13), $R_{arc,a}$ and $R_{arc,b}$ stand for the arc resistance above and below the transit point current respectively. P_a, K_a, K_b, P_b are constants which depend on the length of the electrode gap. As the length of the electrode gap increases, P_a, K_a and K_b increase and P_b decreases.

Implementation and simulation of the DC Arc Model in PSCAD/EMTDC

The DC arc model introduced in this section is based on (3.12) and (3.13). P_a and P_b are assumed as the constant values which are selected from Table 3.2 and Table 3.3, and the DC-CB contact separation time is 100 μs. Based on these assumptions:

• When the DC level is below transit point current ($I_{arc} \leq 100$A)

$$R_{arc,b} = K_{aa} I_{arc}^{-1.283}, \tag{3.14}$$

$$S_a = \frac{K_a}{100}, \tag{3.15}$$

$$K_{aa} = S_a(t - t_0), (K_{aa} \leq K_a). \tag{3.16}$$

• When the DC level is above the current level of transit point($I_{arc} > 100$A)

$$R_{arc,b} = K_{bb} I_{arc}^{-0.736}, \tag{3.17}$$

$$S_b = \frac{K_b}{100}, \tag{3.18}$$

$$K_{bb} = S_b(t - t_0), (K_{bb} \leq K_b). \tag{3.19}$$

In (3.16) and (3.19), t_0 is the time-instant that the DC-CB contact opens. K_a represents the dielectric strength of the electrode gap when contacts separate to its maximum

distance (DC level is under 100A). Similar to K_a, K_b implies the dielectric strength of the electrode gap with the maximum distance of contacts separation when DC level is above 100A. K_{aa} and K_{bb} specify the instantaneous dielectric strength of the electrode gap when the current level is below (above) 100A. S_a (S_b) represents the changing rate of K_{aa} (K_{bb}) when the current is under (above) 100A.

The study system for evaluation of the DC arc model is shown in Fig 3.10. Under a normal condition, the DC-CB is closed. Subsequent to a fault, it opens when the line current reaches 2000A [12]. This system with the same interruption current is also used as the DC study system of Chapter Four and Chapter Five for performance evaluation of the DC-HCBs.

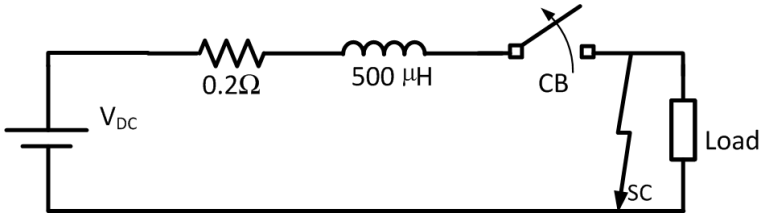

Figure 3.10: A study system of the DC arc model

Table 3.4: Three cases of DC arc model simulations

Case	K_a	K_b
A	662.34	52.63
B	3645.2	293.52
C	50000	2540.79

Table 3.4 provides the values of K_a and K_b for the three study cases. The investigations of the DC arc behaviors, when different dielectric strength of the contact gap are applied, are presented in the following paragraphs.

In Case A, Fig 3.11, K_a and K_b are selected as the dielectric strength of the gap that is not adequate to break the DC. From Fig 3.11 (c), after the contacts of the DC-CB separate at 0.5s, the arc resistance R_{arc} fails to increase to a large value, and results in the arc current I_{arc}, Fig 3.11 (d), increasing until it reaches the maximum current. The arc voltage V_{arc}, Fig 3.11 (b), cannot reach the system voltage because the DC is not interrupted. A small over-voltage is generated by the inductor (V_{ind}), Fig 3.11 (a).

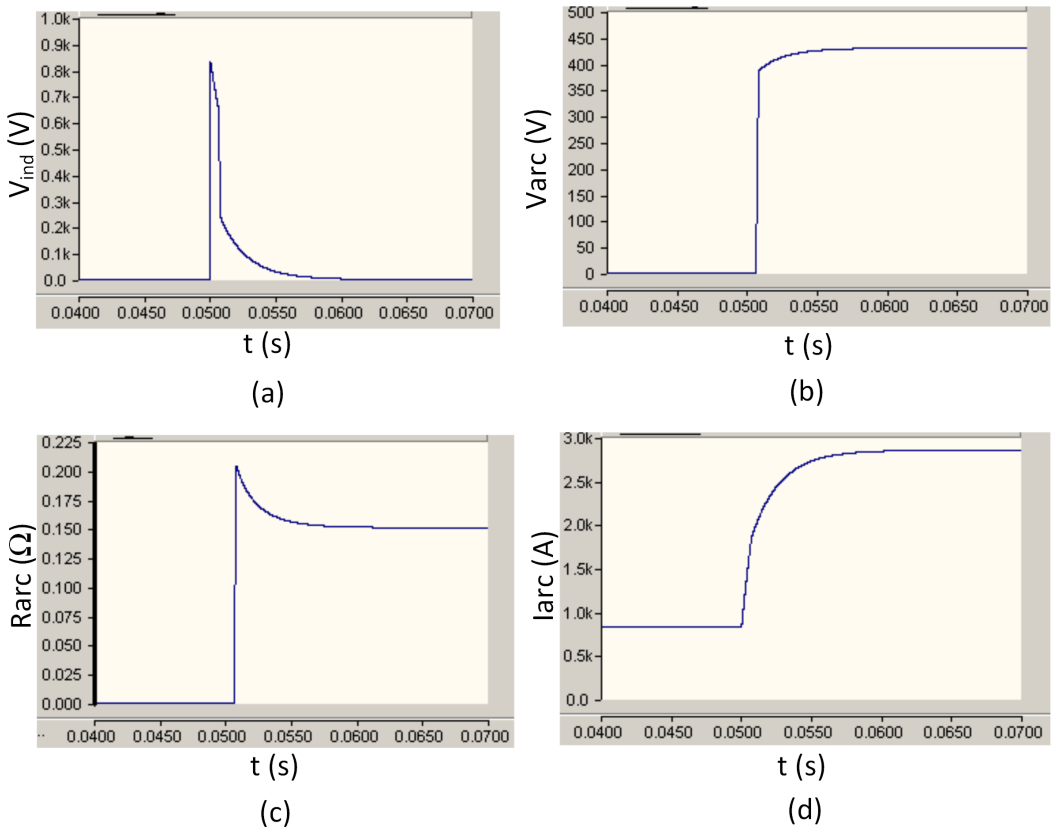

Figure 3.11: DC arc resistance when the dielectric strength of the contacts gap is small, (a) voltage of system inductor (Case A), (b) arc voltage of DC arc model (Case A), (c) arc resistance of DC arc model of Case A, and (d) arc current of DC arc model (Case A).

In Case B, Fig 3.12, K_a and K_b, Table 3.4, are selected as K_{amin} and K_{bmin}. K_{amin} and K_{bmin} are the minimum dielectric strength of the electrode gap with the maximum distance of the contact septation that required to break the DC above and below the transit point current. K_{amin} and K_{bmin} are determined based on a trial and error process that increments K_a and K_b to obtain successful current interruption. In case C, Fig 3.13, a much bigger K_a and K_b are selected, which imply that the dielectric strength of the electric gap is very large.

For both Case B and Case C, the DC fault current is interrupted. Since the study system is highly inductive, the over-voltage generated by the inductor, V_{ind}, is large. The magnitude of this over-voltage is related to the rate of increase of the arc resistance R_{arc}. R_{arc} of Case C, Fig 3.13 (c), increase much faster than that of Case B, Fig 3.12 (c). As a result, a much larger inductor voltage V_{ind} is generated in Case C, Fig 3.13 (a) then Case B, Fig 3.12 (a). Similarly, V_{arc} of Case C, Fig 3.13 (b), is much larger than that

of Case B, Fig 3.12 (b). For the same reason, I_{arc} of Case C, 3.13 (d), reaches its peak value much faster than, I_{arc} of Case B, Fig 3.12 (d). The studies concluded that:

• Opening the MCB of DC interruption without the auxiliary commutation path results in extremely high voltage.

• When K_a and K_b is very large, the MCB performs like a SSCB.

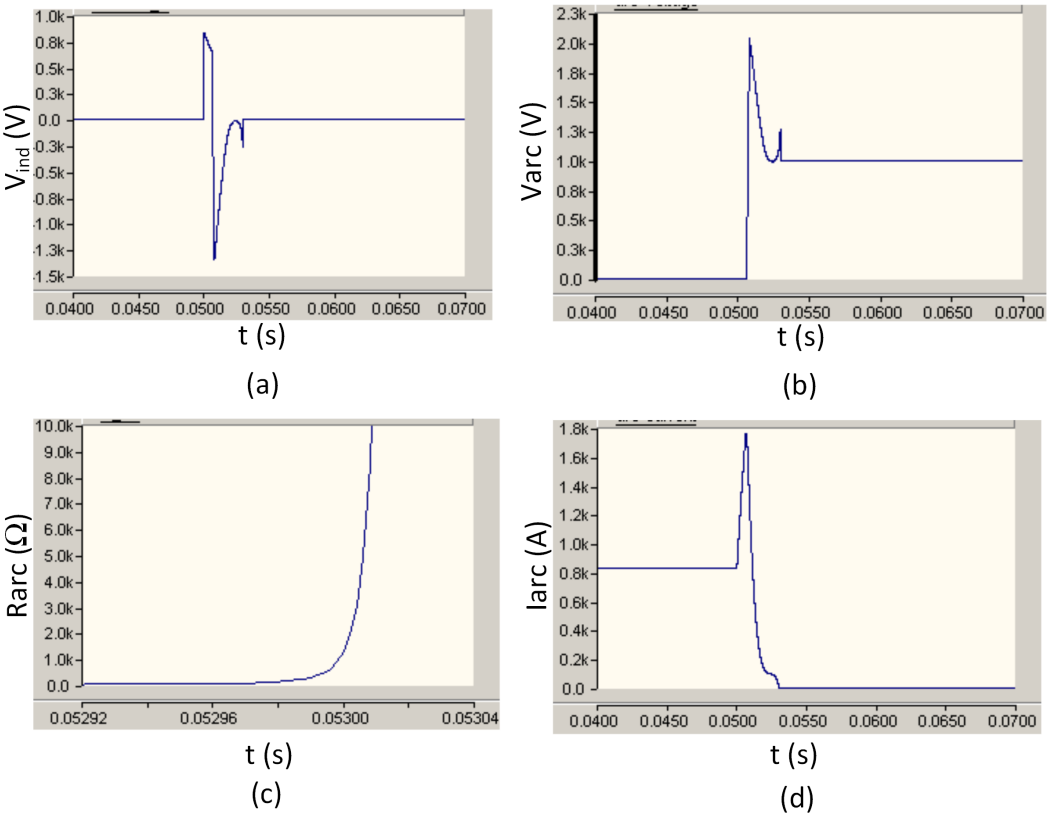

Figure 3.12: DC arc resistance with the minimum dielectric strength of the contacts gap, (a) voltage of system inductor (Case B), (b) arc voltage of DC arc model (Case B), (c) arc resistance of DC arc model of Case B, and (d) arc current of DC arc model (Case B).

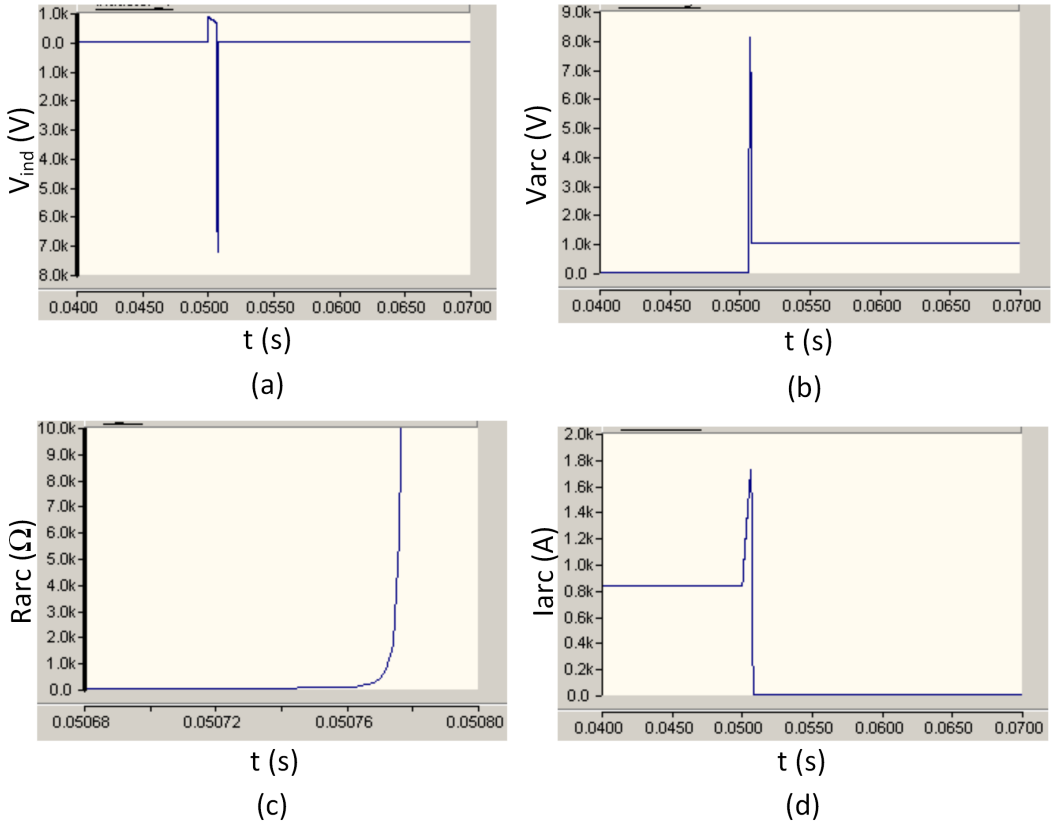

Figure 3.13: DC arc resistance with the much large electrode gap, (a) voltage of system inductor (Case C), (b) arc voltage of DC arc model (Case C), (c) arc resistance of DC arc model of Case C, and (d) arc current of DC arc model (Case C).

3.4 Conclusions

This chapter first introduced the fundamental of the DC arc and then studied the difference between interruption of AC and interruption of DC. Later, two AC arc models, Mayr AC arc model and Cassie AC arc model, were introduced and implemented into the PSCAD/EMTDC platform. Based on these two AC arc models, case studies were carried out in the PSCAD/EMTDC by interrupting the AC either at the instant of the current-zero crossing or at the instant of the maximum (peak) current. From AC arc model simulations, we conclude that it is best to open the CB at the first current zero-crossing when a fault is applied to the system. Section 3.3 studied the DC arc model. The DC arc equations were introduced with focus on the Paukert's empirical arc equation. The DC arc model was developed based on Paukert's empirical arc equation and implemented into the DC study system. Three different "dielectric strength" of arc gap

were simulated. Two cases successfully interrupting the DC and one case fails to interrupt the DC. Based on the DC arc studies, the conclusion is that DC interruption without the auxiliary commutation path is not a practical approach, which results in a high voltage and a long arc time of the CB. In the following chapter, the DC arc model will be implemented into the active mode DC-HCB and the counter-voltage DC-HCB, and K_{amin} of Case B will be used to compare with that of DC-HCBs to evaluate the performance of DC-HCBs.

Chapter 4

Analysis and Simulation of Active Mode DC-HCB

4.1 Introduction

Chapter 3 introduced the DC arc model and the simulation studies were conducted based on implementing a DC-CB without the commutation path into the DC study system. The results show that interrupting the DC using DC-CB without the commutation path is not a practical approach. Therefore, the active mode DC-HCB, which mainly uses a capacitor and a inductor in the commutation path, is introduced to interrupt the DC in this chapter.

This chapter first analyzes the active mode DC-HCB in details without the DC arc model. Then we investigate the dynamic performance of the active mode DC-HCB based on the first current zero-crossing (FCZ) and the second current zero-crossing (SCZ). Section 4.3 studies the active mode DC-HCB considering the DC arc model based on time-domain simulation studies in the PSCAD/EMTDC. By the comparison, the conclusion is that the active mode DC-HCB of the FCZ interruption is superior to that of the SCZ interruption, and thus the active mode DC-HCB of the FCZ interruption will be used to compare with the proposed counter-voltage DC-HCB.

4.2 Analysis of Active Mode DC-HCB

Chapter 2 described the basic concept and the fault-current interruption process of an active mode DC-HCB. In this section, a detailed configuration of an active mode DC-HCB which includes a discharging and pre-charging device is provided, Fig 4.1. The analysis of this section does not include the DC arc model. The fault current interruption is divided into five time intervals. For each time interval, the electric circuit is examined in detail. Table 4.1 introduces the parameters of the DC-HCB of Fig 4.1.

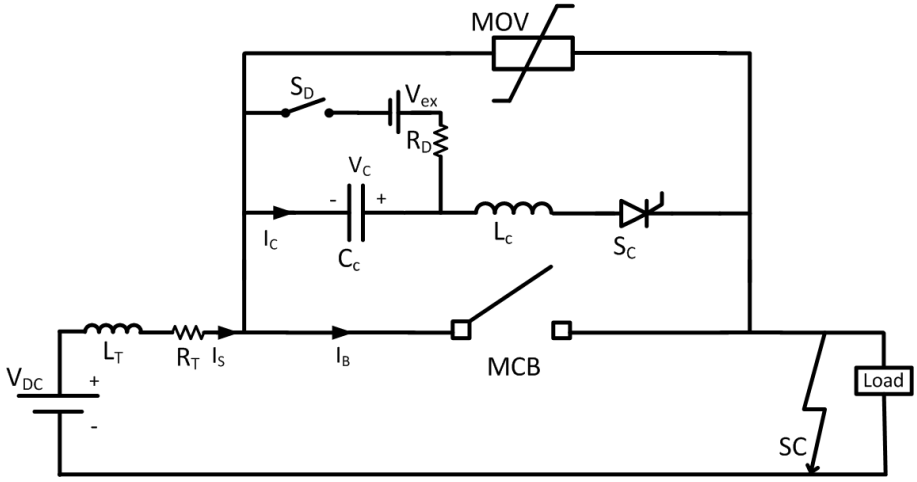

Figure 4.1: Circuit configuration of an active mode DC-HCB

Table 4.1

Parameter name	Parameters symbols
DC Source voltage	V_{DC}
System resistor & System inductor	R_T & L_T
Commutation resistor & Commutation inductor	C_c & L_c
Capacitor Voltage	V_c
Line current	I_s
Main circuit breaker current	I_B
Commutation path current	I_c

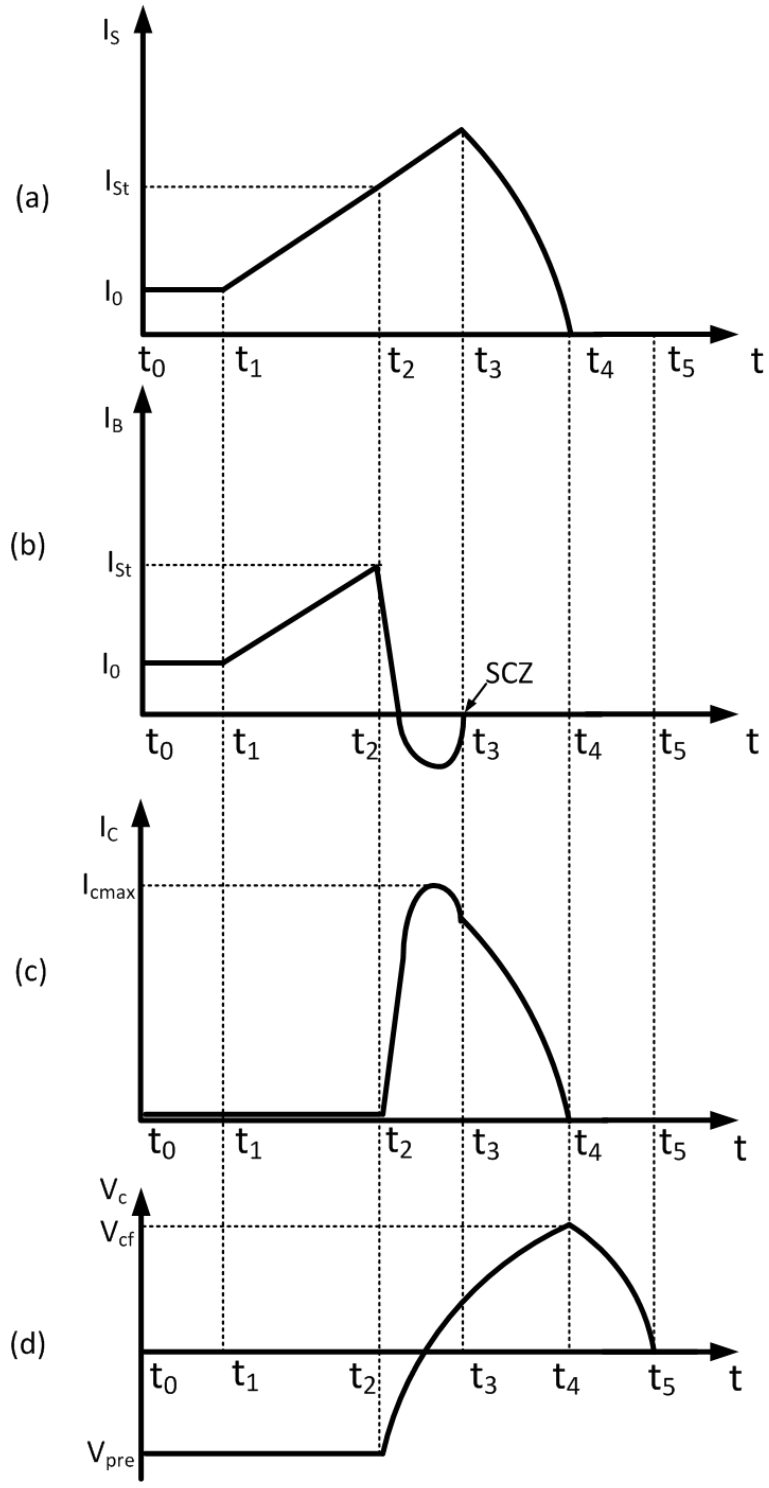

Figure 4.2: The interrupting process of active mode DC-HCB when the MCB opens at the second current zero-crossing (SCZ), (a) line current (I_S), (b) current through the MCB (I_B), (c) commutation current path (I_C), and (d) commutation capacitor voltage (V_c).

4.2.1 Time Intervals for Fault Current Interruption

Chapter 2, Fig 2.2 illustrates the fault interruption process of an active mode DC-HCB based on the first current zero-crossing (FCZ) interruption. Fig 4.2 shows the full sequence of the fault current interruption of an active mode DC-HCB when the mechanical CB operates at the second current zero-crossing (SCZ).

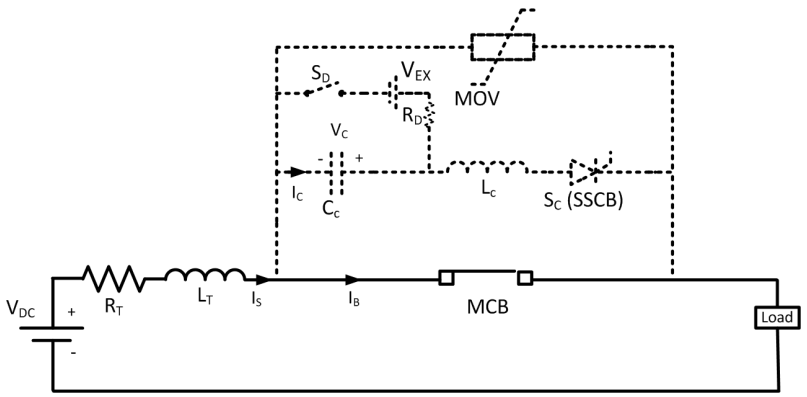

Figure 4.3: First time interval for the fault current interruption

First Time Interval ($t_0 < \mathbf{t} < t_1$)

The first time interval is when the circuit is under normal condition, the line current I_s flows through the MCB and the thyristor S_C is open, Fig 4.3. The system behavior in the first time interval is governed by

$$V_{DC} - I_s(R_T + R_L) = 0. \tag{4.1}$$

In (4.1), V_{DC} represents the system supply voltage and I_s is the line current. R_T and R_L indicate the system resistance and the load resistor and

$$I_0 = \frac{V_{DC}}{R_T + R_L}. \tag{4.2}$$

In this interval, the line current I_s, Fig 4.2 (a), is equal to the current through the MCB, I_B, Fig 4.2 (b),at the rated value of I_0, (4.2). Since the DC-HCB is closed, the commutation current I_c, Fig 4.2 (c), is zero and the commutation capacitor voltage V_c is equal to the pre-charged voltage V_{pre} as shown in Fig 4.2 (d).

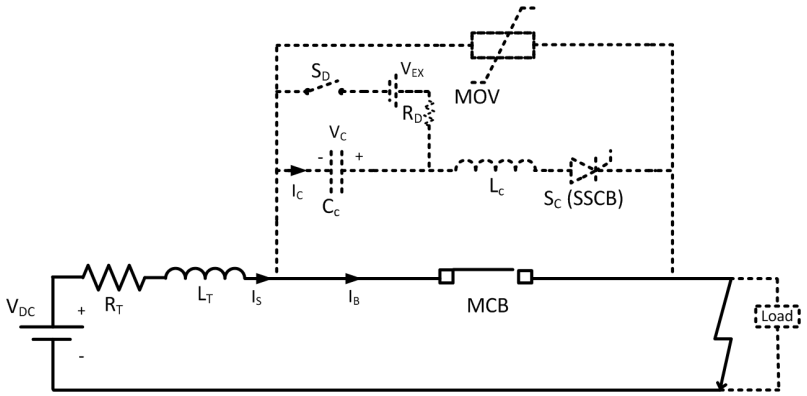

Figure 4.4: Second time interval for the fault current interruption

Second Time Interval ($t_1 < \mathbf{t} < t_2$)

At the beginning of the second time interval, i.e., t = t_1, a fault is applied to the DC system. The DC voltage source is considered as an ideal source and thus V_{DC} remains constant during the fault and the fault current interruption. The system dynamics during the second time interval is generated by

$$V_{DC} = L_T \frac{dI_s(t)}{dt} + R_T I_s(t). \tag{4.3}$$

In general, R_T is small and negligible, the line current I_s, Fig 4.2 (a), which is equal to I_B, Fig 4.2 (b), linearly increases based on

$$\frac{dI_s(t)}{dt} = \frac{V_{DC}}{L_T}. \tag{4.4}$$

Before the fault is applied, the line current I_s is the rated current I_0 which is determined by the R_T and R_L, (4.2). From (4.5)

$$I_s(t) = I_f(1 - e^{-\frac{t}{\tau}}) - I_0 e^{-\frac{t}{\tau}}, \tag{4.5}$$

where

$$\tau = \frac{L_T}{R_T}, \tag{4.6}$$

$$I_f = \frac{V_s}{R_T}. \tag{4.7}$$

τ is the time constant of the system and I_f is the steady-state fault current. Since the load is shorted, the steady-state fault current level is only determined by the system

resistance R_T. Since the MCB is not open, I_c, Fig 4.2 (c), and V_{pre}, Fig 4.2 (d), remain the same as that of the previous interval.

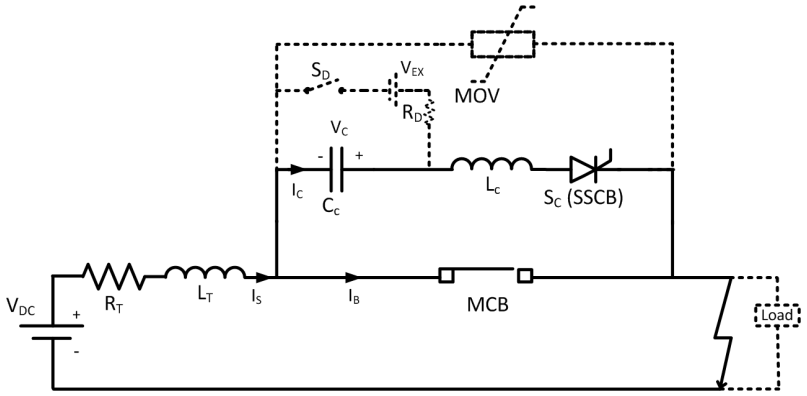

Figure 4.5: Third time interval for the fault current interruption

Third Time Intervals ($t_2 < \mathbf{t} < t_3$)

At the end of the second time interval, i.e., t = t_2, the line current I_s reached to its maximum value I_{St}, the threshold for starting the interrupting process. Thyritor S_C closes instantly and a counter-current, I_c, is injected into the commutation path.

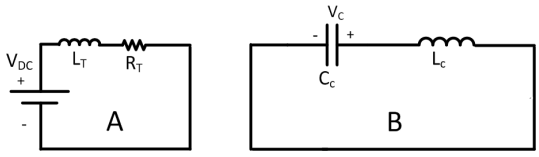

Figure 4.6: Representation of the system of Fig 4.5

It is assumed that the on-state resistance of the MCB is zero. Hence, when the thyristor S_c is closed, the system of Fig 4.5 can be represented by Circuit A and Circuit B in Fig 4.6. The line current I_S of Circuit A, satisfies

$$V_{DC} = L_T \frac{dI_s(t)}{dt} + R_T I_s(t). \tag{4.8}$$

Based on the Circuit B, the commutation capacitor C_c which is pre-charged to V_{pre} discharges its stored energy and transfers the energy to the commutation inductor L_c and thus V_c, Fig 4.2 (d) decreases at the beginning of the interval as governed by

$$V_{pre} + L_c C_c \frac{d^2 V_c(t)}{dt^2} = 0 \; or \; I_{c0} + L_c C_c \frac{d^2 I_c(t)}{dt^2} = 0, \tag{4.9}$$

where $V_c(t)$ represents the commutation capacitor voltage during the interrupting process and I_{c0} is the initial state of the commutation current, which is zero at the beginning of the third time interval. Based on (4.9), the rate of increase of I_c ($\frac{dI_c(t)}{dt}$), the maximum value that I_c could reach (I_{cm}), and the frequency of Circuit B (ω_1) are

$$\frac{dI_c(t)}{dt} = -\frac{V_{c(t)}}{L_c}, \tag{4.10}$$

$$I_{cm} = V_{pre}\sqrt{\frac{C_c}{L_c}}, \tag{4.11}$$

$$\omega_1 = \frac{1}{\sqrt{L_c C_c}}. \tag{4.12}$$

At the beginning of the third interval, the line current, I_s, Fig 4.2 (a), is equal to the commutation current, I_c, and the current through the MCB, I_B, as indicated in 4.13. At the end of the time interval, I_s commutated from I_B to I_c and a current zero-crossing is generated by the MCB, and

$$I_s(t) = I_B(t) + I_c(t). \tag{4.13}$$

By solving (4.8) and(4.9), the line current I_s, the commutation current I_c and the capacitor voltage V_c are

$$I_s(t) = I_f(1 - e^{-\frac{t}{\tau}}) + I_{St}e^{-\frac{t}{\tau}}, \tag{4.14}$$

$$V_c(t) = V_{pre}sin(\omega_1 t), \tag{4.15}$$

$$I_c(t) = \alpha_1 sin(\omega_1 t), \tag{4.16}$$

where

$$\alpha_1 = -\frac{V_{pre}}{\omega_1 L_c}. \tag{4.17}$$

To produce a current zero-crossing in this time interval, the maximum current injected of Circuit B (4.11) must be equal to or greater than the fault current. The appropriate combination of the commutation capacitance C_c and the commutation inductance L_c is needed to guarantee the commutation current I_c can exceed the line current I_s. The MCB could open at either the FCZ or SCZ. The final capacitor voltage at this interval will be the initial condition for the next time interval. When the MCB opens at the FCZ, the capacitor voltage V_c, Fig 2.2 (d), is still negative. This means the counter-current is still being injected at the beginning of the next interval. In this case, the commutation current I_c, Fig 2.2 (c), does not reach the maximum commutation current

value I_{cmax}. However, if the MCB opens at SCZ, the capacitor voltage V_c, Fig 4.2 (d), becomes positive and thus a counter-voltage is produced and the operation is similar to that of the counter-voltage approach. Also, the commutation current I_c, Fig 4.2 (c) reaches I_{cmax} when I_B, Fig 4.2 (b), is interrupted at SCZ.

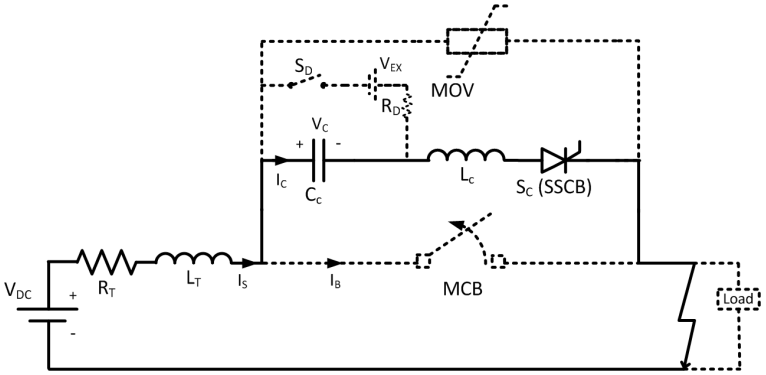

Figure 4.7: Fourth time interval for the fault current interruption

Fourth Time Interval ($t_3 < \mathbf{t} < t_4$)

In this interval, since the contacts of MCB have been separated, there is only one current path for the DC and the RLC circuit is formed, Fig 4.7. Hence, I_s, Fig 4.2 (a), is equal to I_c, Fig 4.2 (c), and I_B, Fig 4.2 (b), remains zero. As the internal source resistance and the commutation resistor are negligible, the total resistance R_{tot} is R_T. The total inductors L_{tot} is the series combination of the system inductance L_T and the commutation inductance L_c. Finally, the total capacitor C_{tot} is the commutation capacitance C_c. At the end of previous time interval, the capacitor voltage was charged to v_{t3} and line current was $i_{s,t3}$. The differential equations with respect to the capacitor voltage for the circuit of Fig 4.7 are,

$$C_c L_{tot} \frac{d^2 V_c(t)}{dt^2} + C_c R_{tot} \frac{dV_c(t)}{dt} + V_c(t) - V_s(t) = 0, \tag{4.18}$$

$$C_c L_{tot} \frac{d^2 i_s(t)}{dt^2} + C_c R_{tot} \frac{di_s(t)}{dt} + i_s(t) = 0. \tag{4.19}$$

Based on (4.18) and (4.19), V_c and I_s are,

$$V_c(t) = V_s + e^{-\alpha_2 t}[bcos(\beta_2 t) - csin(\beta_2 t)], \tag{4.20}$$

$$I_s(t) = e^{-\alpha_2 t}[i_{s,t3}cos(\beta_2 t) - dsin(\beta_2 t)], \tag{4.21}$$

where

$$a = \frac{i_{s,t3}}{C_c}, \tag{4.22}$$

$$b = V_{ct3} - V_s, \tag{4.23}$$

$$c = \frac{1}{\beta_2}(\alpha_2 b + a), \tag{4.24}$$

$$d = \frac{1}{\beta_2}(\frac{b}{L_{tot}} - \alpha i_{s,t3}), \tag{4.25}$$

$$\alpha_2 = \frac{R_{tot}}{2L_{tot}}, \tag{4.26}$$

$$\omega_2 = \frac{1}{\sqrt{L_{tot}C_c}}, \tag{4.27}$$

$$\beta_2 = \sqrt{\omega_2^2 - \alpha_2^2}. \tag{4.28}$$

Since a uni-directional switch is used, the line current cannot flow reversely. At the end of this time interval, the line current reduces to zero and the capacitor is charged to its final voltage V_{cf}, Fig 4.2 (d), based on

$$V_{cf} = V_s + e^{\frac{\alpha_2}{\beta_2}\gamma}[bcos(\frac{-\gamma}{\beta_2}) - bsin(\frac{-\gamma}{\beta_2})]. \tag{4.29}$$

The total time needed for this interval T_4 is given by (4.30),

$$T_4 = \frac{arctan(\frac{1}{\frac{1}{\beta}(\frac{V_{c0}-V_{DC}}{L_T} - \alpha)})}{\beta_2}, \tag{4.30}$$

where

$$\gamma = arctan(-\frac{i_{s,t3}}{d}). \tag{4.31}$$

This time interval has a characteristic similar to those of the third time interval. The total time T_4 is determined by the commutation capacitor C_c, the total inductor L_{tot} and the initial conditions associated with the third interval. If the MCB opens at the FCZ, both I_s and I_c, Fig 2.2 (a) and Fig 2.2 (c), first increase and then reduce to zero at the end of the interval. When I_B is interrupted at the SCZ, I_s (Fig 4.2 (a)) and I_c (Fig 4.2 (c)) directly decrease to zero at the end of the interval.

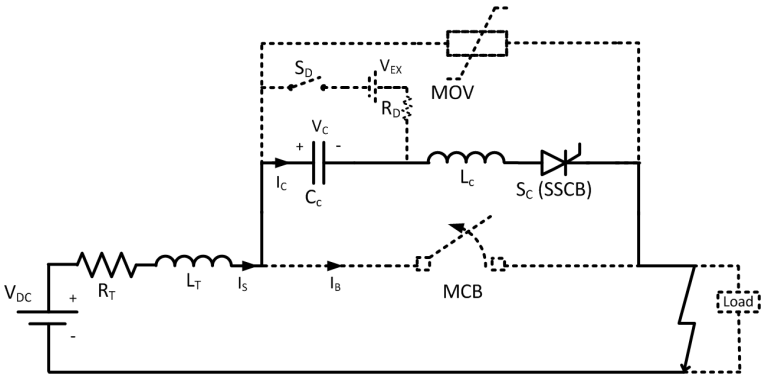

Figure 4.8: Fifth time interval for the fault current interruption

Fifth Time Interval ($t_4 < \mathbf{t} < t_5$)

At the last interval, an external auxiliary voltage source V_{EX}, a switch S_D and a discharging resistor R_D are needed. Since the final voltage of the commutation capacitor has a different polarity than that of the initial pre-charged voltage, the commutation capacitor will be first discharged and then charged to its pre-charged voltage V_{pre}, Fig 4.2 (d). Moreover, because the interruption process is completed, I_s, I_B and I_c are all equal to zero as shown in Fig 4.2.

4.2.2 Dynamic Performance of the Active Mode DC-HCB

In the previous section, we discussed the stages and the associated behavior of the active mode HCB. In this section, we compare the interruption performance of an active mode DC-HCB based on the system and commutation parameters, when the MCB opens at either the FCZ or the SCZ. Comparisons of two current zero-crossings are conducted in four cases, based on the variations of system inductor (L_T), commutation capacitor (C_C), trip current level(I_{St}) and initial pre-charge commutation capacitor voltage (V_{pre}). The frequency of the commutation circuit ω_1 is 1 kHz. In general, ω_1 should be in between a few hundred Hz up to approximately 5000 Hz. If ω_1 is too smaller, the commutation current cannot raise up fast enough to catch up the line current. The upper limit of ω_1 is defined by the detection process and the time for semiconductor switch to change their status. The total energy needed to be absorbed during the interruption process W_{ab} is

$$W_{ab} = \int_{t_0}^{t_5} V_s I_s(t) dt + \frac{1}{2} L_T I_{St}^2 = \frac{1}{2} C_C (V_{cf}^2 - V_{pre}^2). \tag{4.32}$$

W_{ab} can be represented as the summation of the energy stored in the system inductor L_T and the energy needed to dissipated in the DC source. W_{ab} can be also represented as a function of the commutation capacitance C_c, pre-charged capacitor voltage V_{pre} and the final capacitor voltage V_{cf}, (4.32). Fig 4.9 illustrates the total energy stored in the capacitor as a function of the capacitance and the final capacitor voltage by assuming pre-charged capacitor voltage is constant, e.g., 500V. Fig 4.9 shows that higher values of V_{cf} or C_c result in higher dissipated energy W_{ab}.

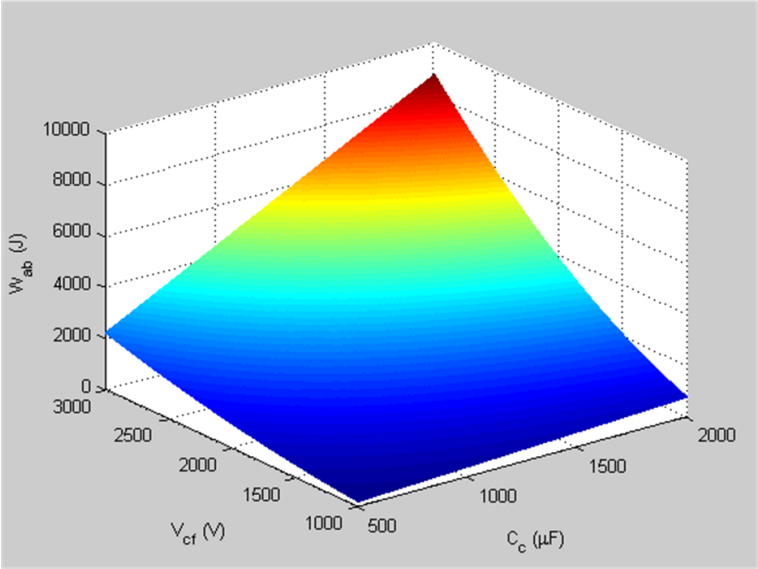

Figure 4.9: The total energy stored in the commutation capacitor, as a function of commutation capacitance and the final capacitor voltage

The effects of C_c, L_T, V_{pre} and I_{St} on the total interruption time (TIT), the final maximum capacitor voltage (V_{cf}), the total energy absorbed by the capacitor (W_{ab}) and the maximum commutation current (I_{cmax}) are shown in Fig 4.10 - Fig 4.13. Case A, Fig 4.10, shows the effect of C_c when it is changed from 500 μF to 2000 μF. In this case, V_{pre} is 1000V, and L_T and R_T are 500 μH and 0.2 Ω. Subsequent to a fault, the thyristor is closed when I_s reaches 2000A. Fig 4.10 (a) shows that, a higher value of C_c, when opening the MCB at either the FCZ or the SCZ, results in a smaller value of V_{cf}. In Fig 4.10 (b), Fig 4.10 (c) and Fig 4.10 (d), increasing the magnitude of C_c results in higher TIT, I_{cmax} and W_{ab} respectively. However, the rate of increase of the I_{cmax} for the SCZ interruption is much faster than that of TIT, V_f and W_{ab}. Hence, from Fig 4.10, we conclude that the active mode DC-HCB of the FCZ interruption is preferred to that of the SCZ interruption.

Case B, Fig 4.11, demonstrates the effect of the system inductor L_T on the performance

of active mode DC-HCB when I_{St} is 2000A. In this case, V_{pre} and C_C are constat at 800V and 500 μF respectively. In Fig 4.11 (c), since both L_c and C_c are constant, I_{cmax} remains unchanged for interrupting at the SCZ. Fig4.11 (c) also illustrates when interrupting I_B at the FCZ, I_{cmax} reduces. Fig 4.11 (a), Fig 4.11 (b) and Fig 4.11 (d) show that, for higher value of ,L_T, the values of V_{cf}, TIT and W_{ab} increase when the MCB is opened at either the FCZ or the SCZ. From Fig 4.11, the value of V_{cf}, TIT and W_{ab} for both current zero-crossing interruptions are very close when L_T changes. However, I_{cmax} of the FCZ decreases significantly while I_{cmax} of SCZ interruption remains constant, when L_T increases. Therefore, from Case B, one conclude that active mode DC-HCB of FCZ interruption is superior to that of the SCZ interruption.

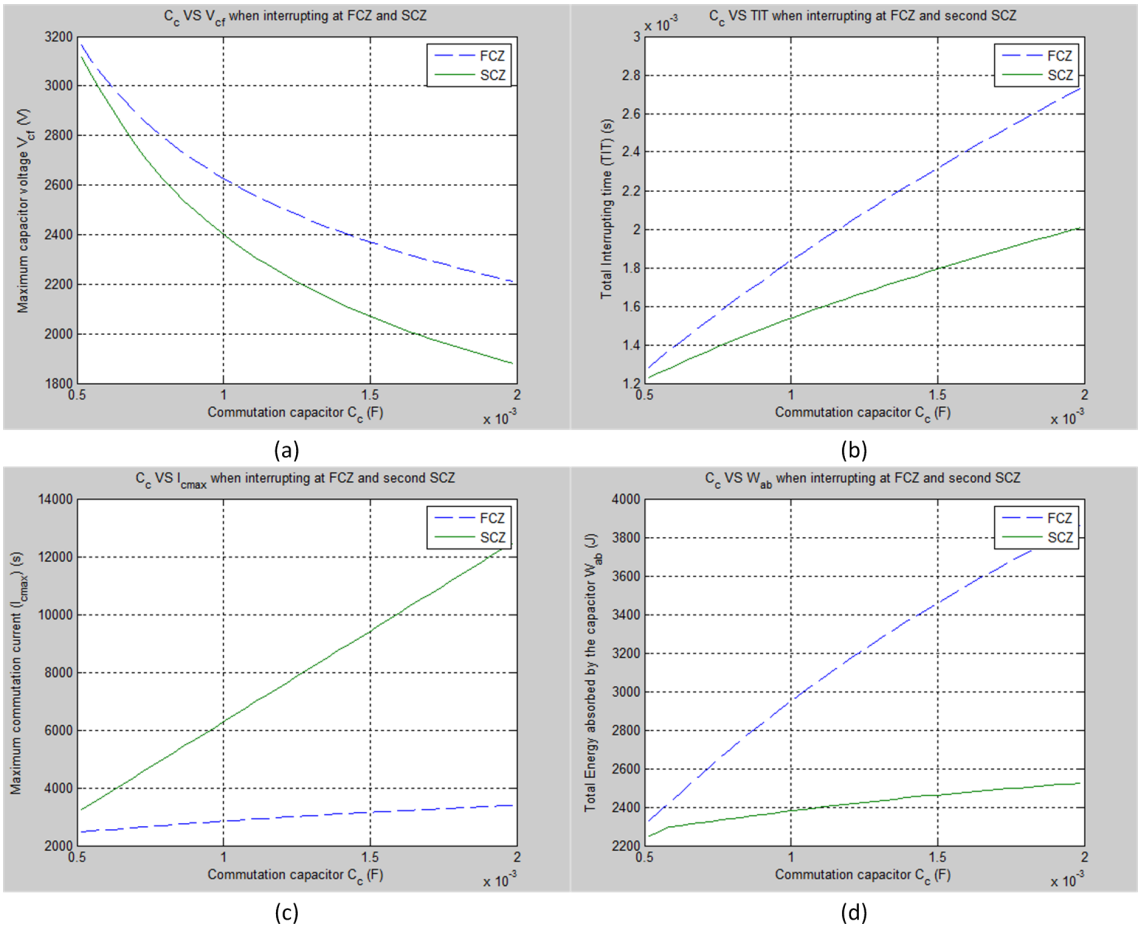

Figure 4.10: Case A, (a) C_c VS V_{cf} when interrupting at the FCZ or at the SCZ, (b)C_c VS TIT when interrupting at the FCZ or at the SCZ, (c) C_c VS I_{cmax} when interrupting at the FCZ or at the SCZ, and (d) C_c VS W_{ab} when interrupting at the FCZ or at the SCZ.

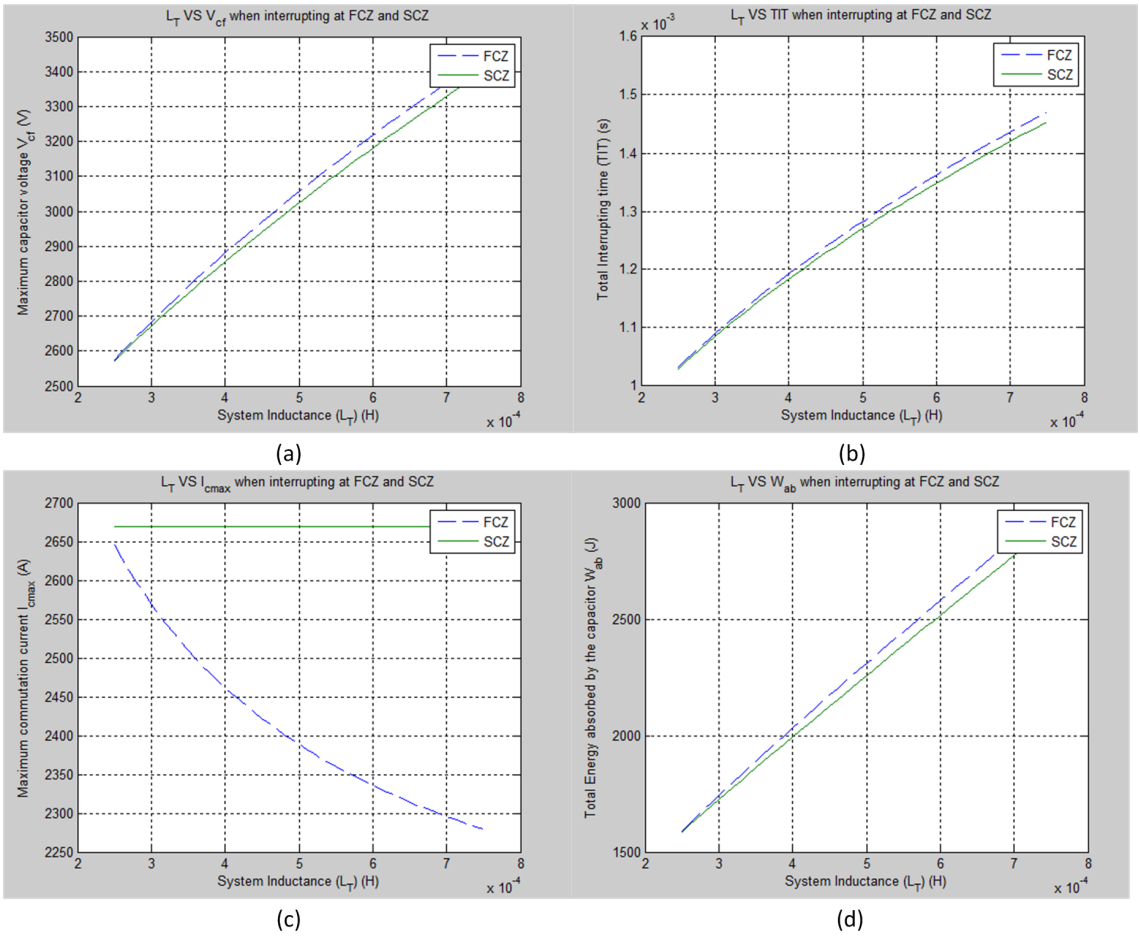

Figure 4.11: Case B, (a) L_T VS V_{cf} when interrupting at the FCZ or at the SCZ, (b)L_T VS TIT when interrupting at the FCZ or at the SCZ, (c) L_T VS I_{cmax} when interrupting at the FCZ or at the SCZ, and (d) L_T VS W_{ab} when interrupting at the FCZ or at the SCZ.

Case C, Fig 4.12, demonstrates the interrupting performance of the active mode DC-HCB when the pre-charged commutation capacitor voltage V_{pre} varies from 700V to 1500V. In this case, L_T, I_{St} and C_c are 500 μH, 2000 A and 800 μF. From Fig 4.12 (a) and Fig 4.12 (c), a smaller value of V_{pre} leads to a smaller magnitude of V_{cf} and I_{cmax}. Fig 4.12 (b) and Fig 4.12 (d) illustrate that a larger value of V_{pre} results in greater values of TIT and W_{ab} when I_B is interrupted at the FCZ. In contrast, larger values of V_{pre} result in smaller values of TIT and W_{ab} when the MCB opens at the SCZ. From Fig 4.12, variation of V_{pre} results in relatively small changing of V_{cf}, TIT and W_{ab} compare to that of I_{cmax}. A higher value of V_{pre} results in an extremely larger value of I_{cmax} of the SCZ interruption. Therefore, the active mode DC-HCB of FCZ interruption is the preferred choice as compared with the SCZ interruption in Case C.

Case D, Fig 4.12, shows the effect of the trip level current I_{St}, from 1000A to 3000A, on the V_{cf}, TIT, I_{cmax} and W_{ab} when C_c, L_T and V_{pre} remain unchanged. Fig 4.13 shows that:

• Increasing I_{St} increases the values of V_{cf} and W_{ab} for both the FCZ and the SCZ interruption, Fig 4.13 (a)and Fig 4.13 (d).

• As I_{St} increases, I_{cmax} remains constant when interrupting the I_B at the SCZ, but I_{cmax} increases when the MCB opens at the FCZ, Fig 4.13 (c).

• A higher value of I_{St} leads to a smaller value of TIT when interrupting the current at the zero-crossings, Fig 4.13 (b).

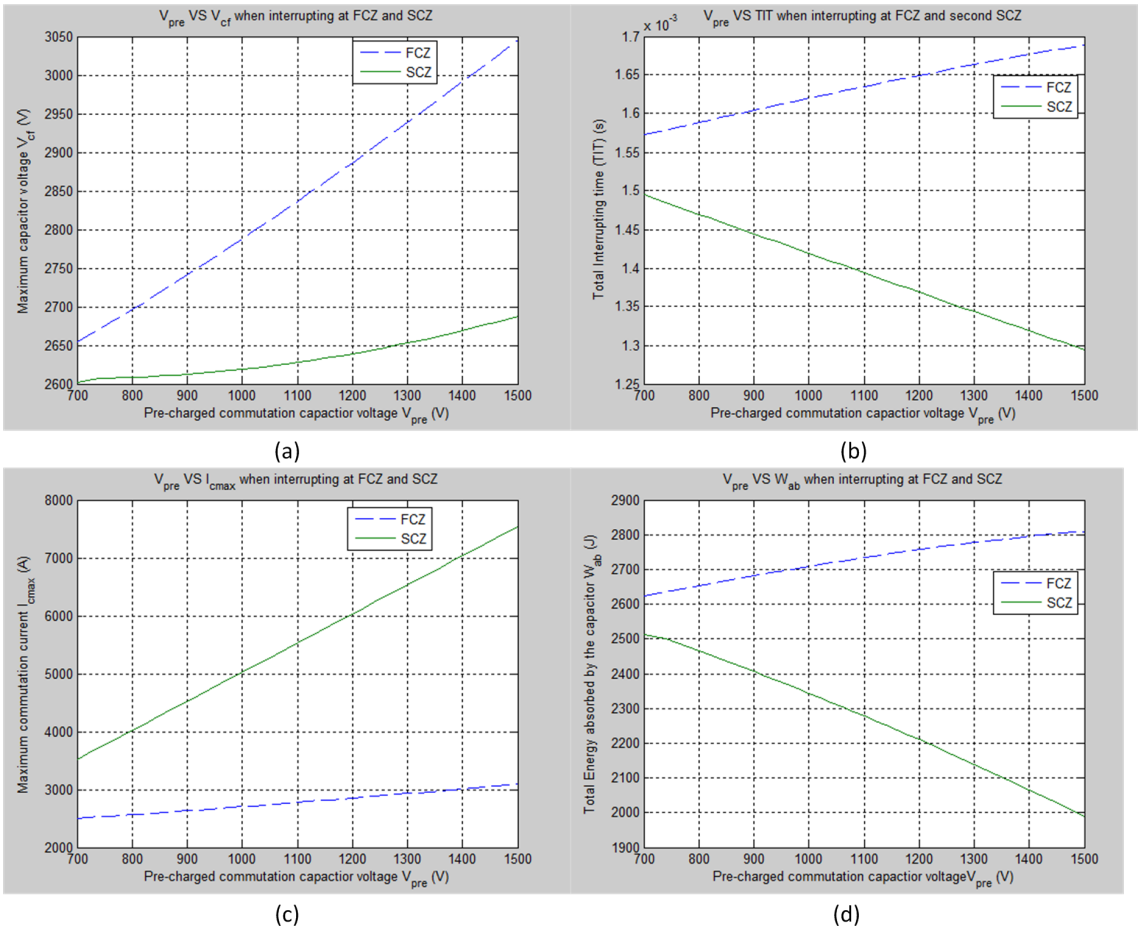

Figure 4.12: Case C, (a) V_{pre} VS V_{cf} when interrupting at the FCZ or at the SCZ, (b)V_{pre} VS TIT when interrupting at the FCZ or at the SCZ, (c) V_{pre} VS I_{cmax} when interrupting at the FCZ or at the SCZ, and (d) V_{pre} VS W_{ab} when interrupting at the FCZ or at the SCZ.

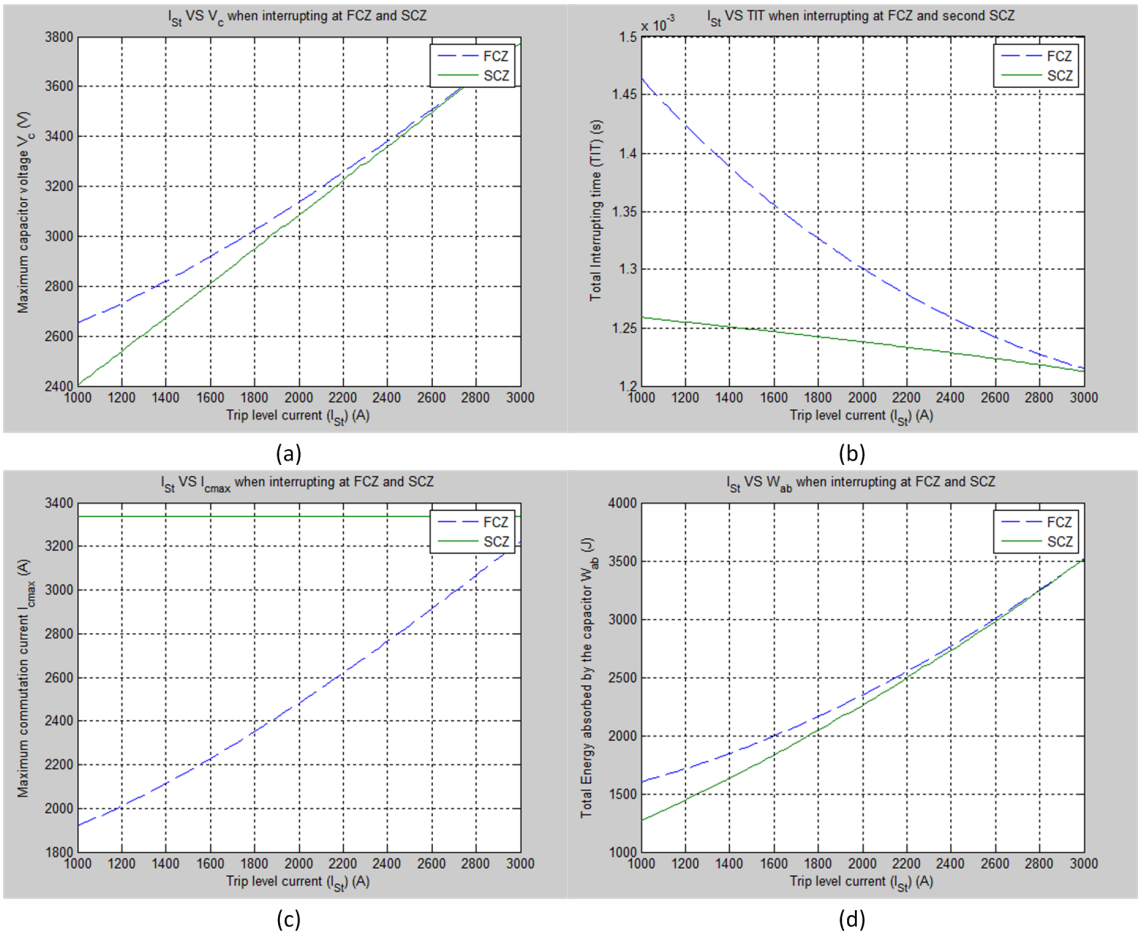

Figure 4.13: Case D, (a) I_{St} VS V_{cf} when interrupting at the FCZ or at the SCZ, (b)I_{St} VS TIT when interrupting at the FCZ or at the SCZ, (c) I_{St} VS I_{cmax} when interrupting at the FCZ or at the SCZ, and (d) I_{St} VS W_{ab} when interrupting at the FCZ or at the SCZ.

From Fig 4.10 to Fig 4.13, we observed that, when the MCB opens at the SCZ, the TIT, V_{cf} and W_{ab} are slightly lower than those values when the MCB opens at the FCZ. However, I_{cmax} is much higher when the MCB opens at the SCZ in general. Therefore, interrupting the DC at the FCZ is the preferred choice for the active mode DC-HCB.

4.3 Impact of DC arc

From previous section, we concluded that interrupting the DC at the FCZ is the preferred option. This section conduct the simulation studies of the active mode DC-HCB considering the DC arc model. The propose of PSCAD/EMTDC simulation studies are to examine the effect of implementing DC arc model, from Chapter 3, on the performance

of the active mode DC-HCB. Different values of dielectric strength of the contact gap K_a are examined. This study concludes that analysing the active mode DC-HCB without the DC arc model is a valid approximation. Also the minimum dielectric strength K_{amin} when the MCB opens at either the FCZ or the SCZ is determined. Based on K_{amin}, we conclude that the active mode DC-HCB of the FCZ interruption is superior to that of the SCZ interruption. Finally, we compare the K_{amin} of FCZ interruption with that of the DC-CB without the commutation path to evaluate the performance of the active mode DC-HCB.

Table 4.2: Comparisons of analytical results (Section 4.2) with simulation results (Section 4.3)

Type	V_{cf} (V)	TIT (μs)	W_{ab} (J)	$I_{cmax}(A)$
An active mode DC-HCB of the FCZ interruption				
analytic	2409.74	1.740	2778.4	2469.22
$K_{amin} = 178.24$	2386.23	1.704	2723.2	2999.31
$K_a = 800$	2496.96	1.725	2747.2	2726.31
$K_a = 4000$	2407.65	1.738	2772.5	2469.22
An active mode DC-HCB of the SCZ interruption				
analytic	2381.62	1.694	2711.05	3098.93
$K_{amin} = 4863.62$	2380.41	1.697	2708.15	3098.93

The DC study system used in this section is the same as that of Chapter 3, Fig 3.10. The system inductance L_T and the system resistance R_T are 500 μH and 0.2 Ω respectively. The commutation capacitance C_c and the pre-charged voltage V_{pre} are 1000 μF and 500 V. The frequency of the commutation circuit is 1000Hz and the trip current level is 2000A. The MCB is considered as a switch with its the operation time of 100 μs. Table 4.2 summarizes both analytical results of Section 4.2 and simulation results of this section.

For interrupting the DC at the FCZ, four sets of data are provided in Table 4.2. The first set (first row) of data shows the analytical results based on equations of Section 4.2. The second set of data provides the simulation results when dielectric strength of the gap K_a is equal to the minimum dielectric strength of the gap K_{amin}. The last two sets of data offer the simulation results as K_a is larger than K_{amin}. For interrupting the DC at the SCZ, only two sets of data are provided. These two sets of data are the same type of data as the first two sets of data provided for interrupting the DC at the FCZ. Table 4.2 shows that K_{amin} of interrupting the DC at FCZ is much less than that of interrupting at SCZ.

Therefore, the first conclusion is that the active mode DC-HCB of the FCZ interruption is superior to that of the SCZ interruption. By comparing the simulation results of the FCZ interruption, a smaller value of K_a leads to a lower magnitude of TIT. However, the TIT of the FCZ interruption is always higher than that of the SCZ interruption. From Table 4.2, a lower value of K_a also results in a larger value of I_{cmax}, but I_{cmax} of the SCZ interruption is always larger than that of the FCZ interruption . Table 4.2 also depicts that increasing K_a leads to a smaller value of V_{cf}. This means that DC arc dissipates less power as K_a increases. Fig 4.14 and Fig 4.15 illustrate the simulation waveforms when K_a is 178.24 and 800 respectively.

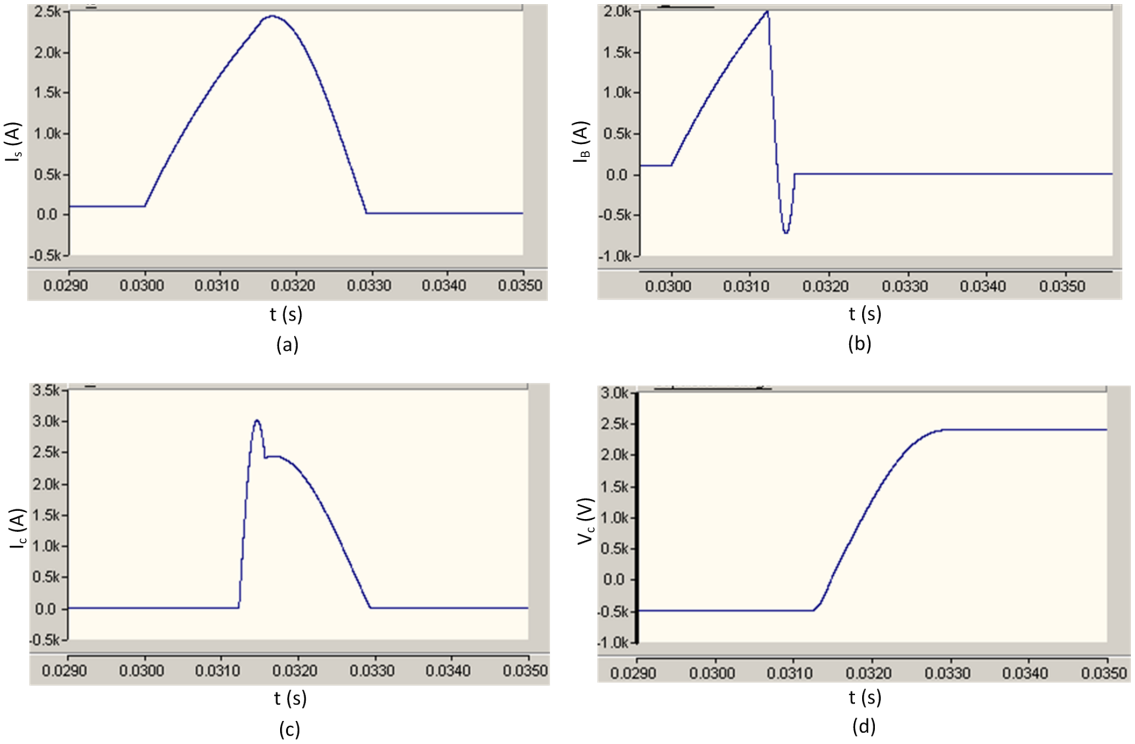

Figure 4.14: Simulation waveforms of the active mode DC-HCB of the FCZ interruption when K_a is 178.2, (a) I_s vs t, (b) I_B vs t, (c) I_c vs t, and (d) V_c vs t.

Based on Fig 4.14 and Fig 4.15, higher values of K_a result in smaller values of I_B, Fig 4.14 (b) and Fig 4.15 (b), and thus lead to lower values of I_c, Fig 4.14 (c) and Fig 4.15 (d). By implementing the DC arc model, I_s of Fig 4.14 (a) and Fig 4.15 (a) and V_{cf} of Fig 4.14 (d) and Fig 4.15 (d) exhibit insignificant changes. Overall, when interrupting the DC at the FCZ considering the DC arc, the performance of the active mode DC-HCB is in between the performance of interrupting the DC at the FCZ excluding the DC arc model and interrupting the DC at the SCZ without considering the DC arc. If the dielectric strength of the gap is low (K_a is small, but larger than K_{amin}), the MCB opens at the

FCZ but the DC is interrupted at the SCZ. In this case, the active mode DC-HCB of the FCZ interruption performs similar to the active mode DC-HCB of the SCZ interruption without considering the DC arc model. If K_a is larger (much larger than K_{amin}), the active mode DC-HCB of the FCZ interruption, with DC arc model, performs similar to the active mode DC-HCB of the FCZ interruption without considering the DC arc model. Hence, the analysis of the active mode DC-HCB excluding the DC arc model is a valid approximation and can be adopted for performance studies of the active mode DC-HCB.

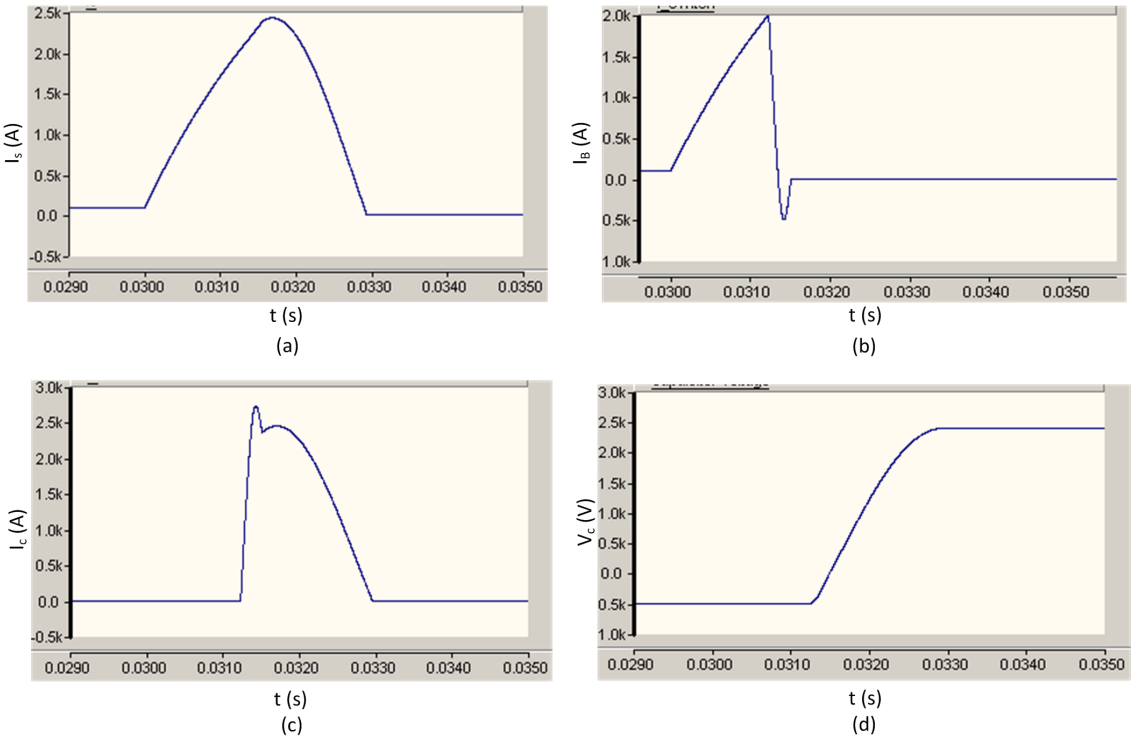

Figure 4.15: Simulation waveforms of the active mode DC-HCB of the FCZ interruption when K_a is 178.2, (a) I_s vs t, (b) I_B vs t, (c) I_c vs t, and (d) V_c vs t.

At last, we compare the active mode DC-HCB of the FCZ interruption with he DC-CB without the commutation path in Chapter Three. In Fig 3.12 and Table 3.4 of Chapter three, the DC-CB without the commutation circuit requires K_{amin} to be 3645.2. Moreover, the DC-CB without the commutation circuit results in large over-voltage across the inductor and long arcing time. In contrast, the active mode DC-HCB of FCZ interruption only needs K_{amin} to be 178.24, Table 4.2. Furthermore, most of the energy is absorbed by the communion capacitor and the acing time is relatively short compared to that of the DC-CB without the commutation circuit. Therefore, the active mode DC-HCB with FCZ interruption is superior to the DC-CB without the commutation circuit

4.4 Conclusion

In this chapter, we first described the active mode DC-HCB operation without considering the DC arc model. Based on the analysis, we discussed the interruption stages based on the active mode DC-HCB, and then investigated the dynamic performance of the active mode DC-HCB based on the FCZ interruption and the SCZ interruption. From this section, the conclusion is that the active mode DC-HCB of FCZ interruption is preferred to that of the SCZ interruption. The reason is that I_{cmax} of the SCZ interruption is much larger that of the FCZ interruption, while V_f, TIT and W_{ab} are comparable, respectively. The time-domain simulation studies also include of the DC arc model. From the PSCAD/EMTRC simulation results, we also conclude that the active mode DC-HCB of the FCZ interruption is preferred to that of the SCZ interruption. This is because the K_{amin} of the active mode DC-HCB of the FCZ interruption is much lower than that of the active mode DC-HCB of the SCZ interruption. Also, the active mode DC-HCB of the FCZ interruption is superior to the DC-CB without the commutation path. Hence, the active mode DC-HCB of the FCZ interruption will be compared with the behavior of the proposed counter-voltage DC-HCB in chapter 6.

Chapter 5

Analysis and Simulation of Counter-Voltage DC-HCBs

5.1 Introduction

Chapter 4 presented the active mode DC-HCB, which is a current commutation based DC-HCBs for DC interruption. In this chapter, two different counter-voltage DC-CBs, referred to the traditional counter-voltage (TCV) DC-HCB and the alternative counter-voltage (ACV) DC-HCB are introduced.

The two DC-HCB configurations are analysed in details. The analysis discusses the interruption stages of both DC-HCBs. The study of Section 5.3 focuses on the dynamic performance of TCV DC-HCB and ACV DC-HCB. Section 5.4 provides the PSCAD/EMTDC simulation results of both counter-voltage DC-HCBs, including the DC arc model. The studies conclude that the performance of the proposed ACV DC-HCB is superior to that of (i) the TCV DC-HCB, and (ii) the DC-CB without commutation path. Hence, the proposed ACV DC-HCB performance is compared with the active mode DC-HCB (Chapter 4) with the FCZ interruption in Chapter 6.

5.2 Analysis of Counter-Voltage DC-HCBs

Chapter two described the basic concepts and the sequence of actions of the fault current interruption process of both the TCV DC-HCB and the ACV DC-HCB. In this section, a detailed analysis of interruption stages with the associated models for each of the

counter-voltage DC-HCB is presented.

5.2.1 Analysis of the TCV DC-HCB

Fig 5.1 shows a detailed circuit diagram of a TCV DC-HCB and Fig 5.2 illustrates its fault current interruption process. The process is divided into four time intervals. The interruption process associated with each time interval are described in the following sections and Table 5.1 introduces the parameters.

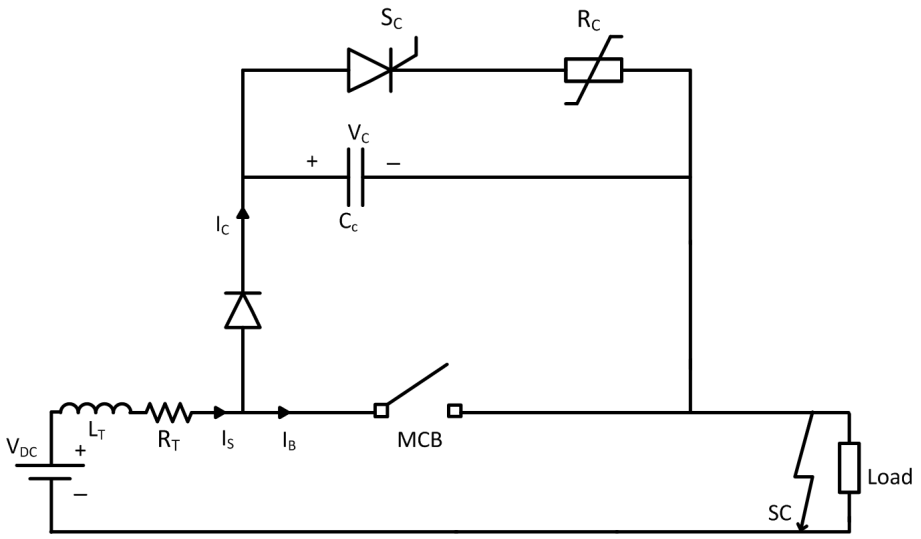

Figure 5.1: Configuration of a TCV DC-HCB

Table 5.1

Parameter name	Parameters symbols
Source voltage	V_{DC}
System resistor & System inductor	R_T & L_T
Commutation capacitance & Capacitor Voltage	C_c & V_c
Line current	I_s
Commutation current	I_c
Current through the MCB	I_B

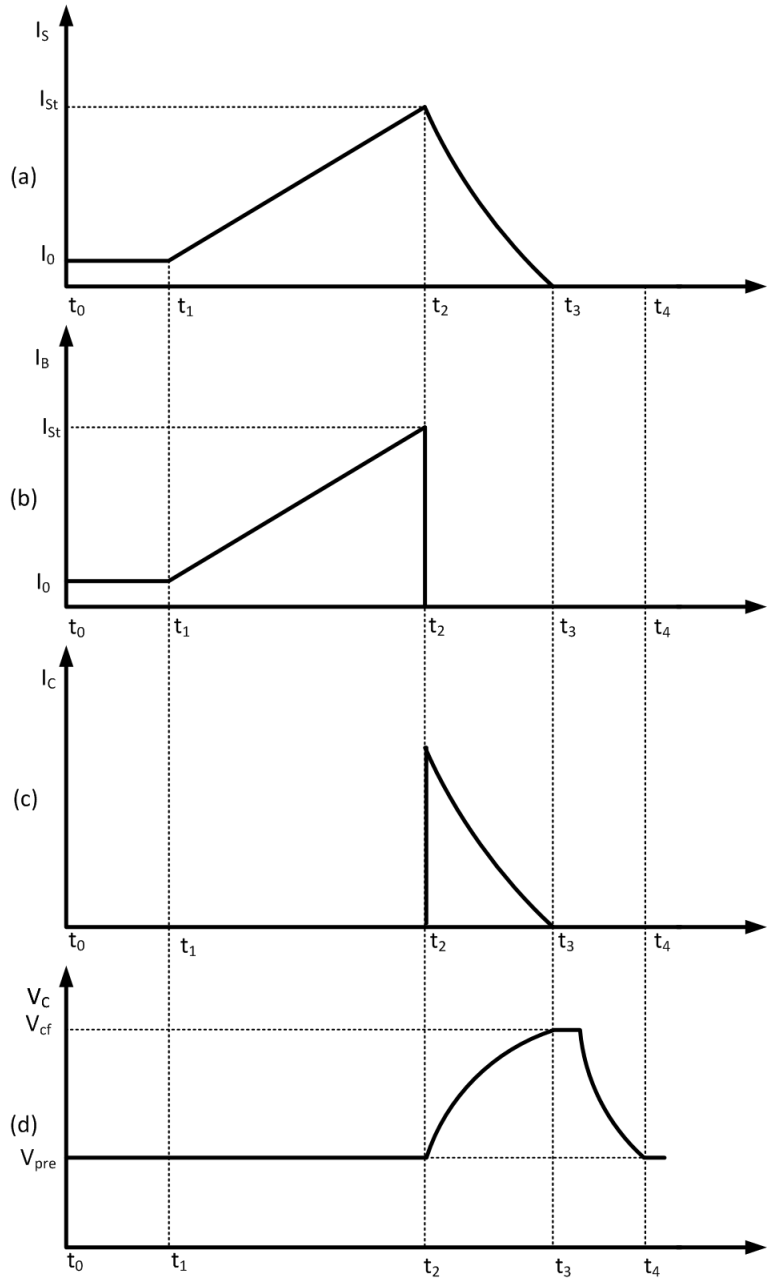

Figure 5.2: The interruption process of the TCV DC-HCB, (a) line current (I_S) (b) current through the MCB (I_B), (c) commutation current path (I_C), and (d) commutation capacitor voltage (V_c).

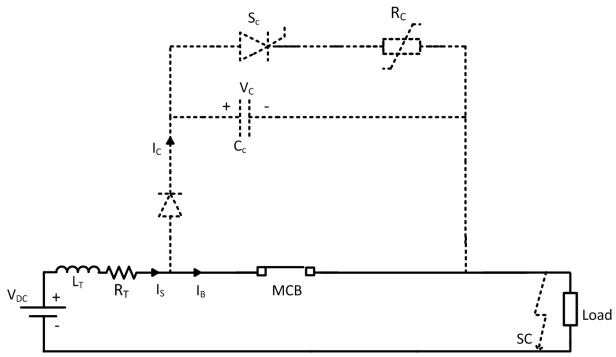

Figure 5.3: Circuit configuration of the TCV DC-HCB during the first time interval

First Time Intervals ($t_0 < \mathbf{t} < t_1$)

In the first time interval, the system is under a normal condition, Fig 5.3. The line current I_s flows through the MCB and the diode block the current flow in the commutation capacitor. The system behavior during the first interval is provided by

$$V_{DC} - I_s(R_T + R_{on} + R_L) - L_T \frac{di}{dt} = 0, \tag{5.1}$$

where R_L is the load resistance, R_T is the system resistance and R_{on} stands for the on-state resistance of the MCB. Since R_{on} is small and negligible, (5.1) can be approximated by

$$I_0 = \frac{V_{DC}}{R_T + R_L}. \tag{5.2}$$

In the first interval, the line current I_s, Fig 5.2 (a), is equal to the current through the MCB I_B, Fig 5.2 (b). I_c, Fig 5.2 (c), is zero and the magnitude of the commutation capacitor voltage V_c, Fig 5.2 (d) is V_{pre}.

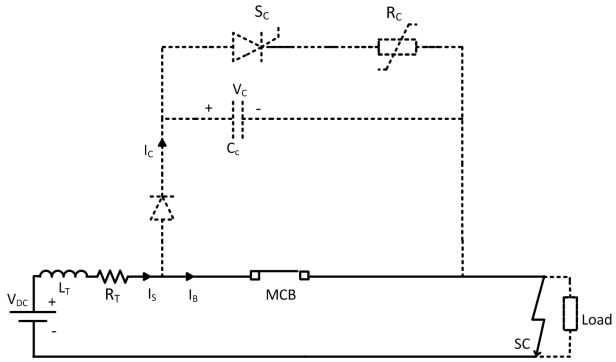

Figure 5.4: Circuit configuration of the TCV DC-HCB during the second time interval

Second Time Intervals ($t_1 < \mathbf{t} < t_2$)

In the second time interval, a fault is applied to the DC system by shorting the load terminal. Since the DC source is considered an ideal source, V_{DC} remains constant during the fault and the fault interruption interval. The system dynamics of the second time interval are governed by

$$V_{DC} = L_T \frac{dI_s(t)}{dt} + R_T I_s(t). \tag{5.3}$$

Compared to the voltage of the inductor, the voltage across R_T is small and thus it can be neglected. Hence, the line current I_s, Fig 5.2 (a), which is equal to I_B, Fig 5.2 (b), linearly increases based on

$$\frac{dI_s(t)}{dt} = \frac{V_{DC}}{L_T}. \tag{5.4}$$

By solving (5.3), the line current I_s of second time interval is

$$I_s(t) = I_f(1 - e^{-\frac{t}{\tau}}) - I_0 e^{-\frac{t}{\tau}}, \tag{5.5}$$

where

$$\tau = \frac{L_T}{R_T}, \tag{5.6}$$

$$I_f = \frac{V_{DC}}{R_T}. \tag{5.7}$$

τ is the time constant of the system and I_f is the steady-state fault current. During the second time interval, the MCB does not open. Therefore I_c, Fig 5.2 (c), and V_{pre}, Fig 5.2 (d), are the same as those of the previous interval.

Third Time Intervals ($t_2 < \mathbf{t} < t_3$)

In the third interval, the interruption process starts. At the beginning of this interval, the line current I_s is at the trip level, I_{St}, the threshold for starting the interruption process. The MCB receives the opening signal and thus the line current starts flowing into the commutation capacitor C_c. The commutation capacitor is pre-charged which imposes a counter-voltage to oppose the current flow and thus the line current starts to

drop. This is accompanied by charging C_c as shown in Fig 5.11 (d). Since the DC arc of the MCB is not considered, I_B, Fig 5.2 (b) instantly dropped to zero when the MCB opens. Hence, the line current I_s, Fig 5.2 (a) is the same as the commutation current I_c, Fig 5.2 (c), after the MCB opens. The dynamics of the third time interval are governed by

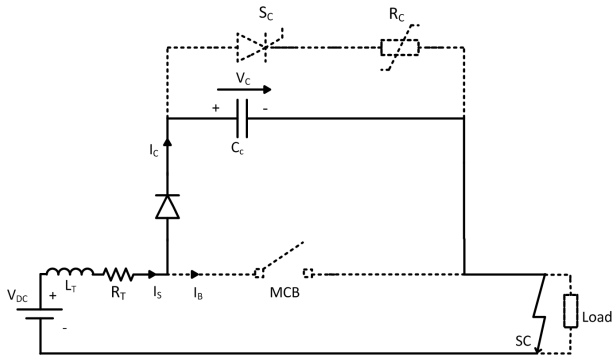

Figure 5.5: Circuit configuration of the TCV DC-HCB during the third time interval

$$V_{DC} - I_s(t)R_T - V_c(t) - L_T\frac{dI_s(t)}{dt} = 0, \tag{5.8}$$

$$I_c = C\frac{dV_c}{dt}. \tag{5.9}$$

Based on (5.8) and (5.9),

$$\begin{bmatrix} \dot{I_s}(t) \\ \dot{V_c}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_T}{L_T} & \frac{1}{L_T} \\ \frac{1}{C_c} & 0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_T} \\ 0 \end{bmatrix}, \tag{5.10}$$

$$\begin{bmatrix} I_{s0} \\ V_{c0} \end{bmatrix} = \begin{bmatrix} I_{St} \\ V_{pre} \end{bmatrix}. \tag{5.11}$$

By solving (5.10) and (5.11), the line current I_s and V_c are given as

$$V_c(t) = V_{DC} + e^{-\alpha t}[(V_{c0} - V_{DC})cos(\beta t) - \frac{1}{\beta}(\alpha(V_{c0} - V_{DC}) + \frac{I_{s0}}{C_c})sin(\beta t)], \tag{5.12}$$

$$I_s(t) = e^{-\alpha t}[I_{s0}cos(\beta t) - \frac{1}{\beta}(\frac{V_{c0} - V_{DC}}{L_T} - \alpha I_{s0})sin(\beta t)], \tag{5.13}$$

where

$$\alpha = \frac{R_T}{2L_T}, \tag{5.14}$$

$$\omega = \frac{1}{\sqrt{L_T C_c}}, \tag{5.15}$$

$$\beta = \sqrt{\omega^2 - \alpha^2}. \tag{5.16}$$

Normally, the system resistor R_T is small. Therefore, the magnitude of ω is much larger than the magnitude of α, and the value of β is dominated by ω. As the capacitor voltage (V_c) charges to the maximum voltage (V_f), the line current I_s decreases to zero at t_3. Because the diode only allows one directional current flow, the commutation current I_c cannot flow reversely, and thus the capacitor cannot be discharged until the energy dissipation process starts. At the end of time interval t_3, the energy stored in the inductor transfers to the commutation capacitor. Based on (5.12) and (5.13), the final voltage of capacitor V_f and time interval T_3 are

$$V_f = V_{DC} + (V_{c0} - V_s)e^{\frac{\alpha}{\beta}\gamma}[cos(\frac{\gamma}{\beta}) - sin(\frac{\gamma}{\beta})], \tag{5.17}$$

$$T_3 = \frac{arctan(\frac{1}{\frac{1}{\beta}(\frac{V_{c0}-V_{DC}}{L_T} - \alpha)})}{\beta}, \tag{5.18}$$

where

$$\gamma = arctan(\frac{I_{s0}}{\frac{1}{\beta}(\frac{V_{c0}-V_{DC}}{L_T} - \alpha I_{s0})}). \tag{5.19}$$

For the TCV DC-HCB, the total interruption time(TIT) of TCV DC-HCB is equal to the time interval T_3.

Fourth Time Intervals ($t_3 < \mathbf{t} < t_4$)

The last time interval, is the discharging process of the TCV DC-HCB as shown in Fig 5.12. After t_3, a closing signal is sent to the commutation switch S_c and then the capacitor starts to discharge. When the capacitor is discharged to a pre-charged voltage level, S_c turns off and the discharging process ends at t_4. The total energy to be dissipated (W_T)

is

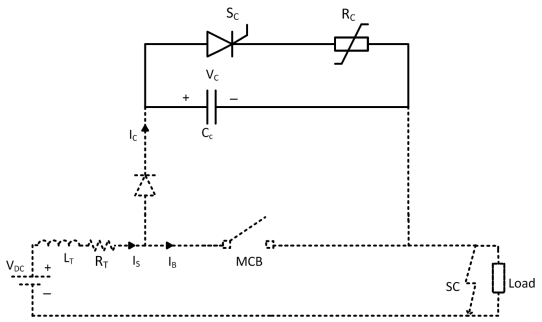

Figure 5.6: Circuit configuration of the TCV DC-HCB during the fourth time interval

$$W_T = \frac{1}{2}L_T I_s^2 + \int_{t_0}^{t_3} V_{DC} I_s dt = \frac{1}{2}C_c(V_f^2 - V_{pre}^2). \tag{5.20}$$

When the interruption process is completed, I_s, Fig 5.2 (a), I_B, Fig 5.2 (b), and I_c, Fig 5.2 (c), are zero. The voltage of the capacitor V_c, Fig 5.2 (d), drops from V_f to V_{pre} in the fourth interval.

5.2.2 Analysis of the ACV DC-HCB

The configuration of the ACV DC-HCB is shown in Fig 5.7. The operation time of the MCB is considered in the ACV DC-HCB current interruption, Fig 5.8. The fault interruption process is divided into seven intervals and discussed in the following paragraphs. The discharging device is a resistor R_c, Fig 5.7. Table 5.2 introduces the parameters of the DC-HCB in Fig 5.7.

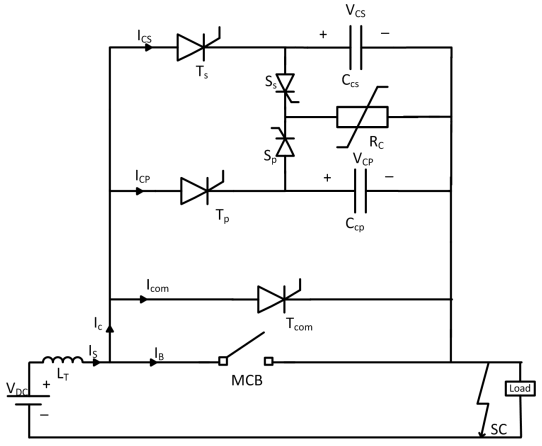

Figure 5.7: Circuit configuration of the ACV DC-HCB

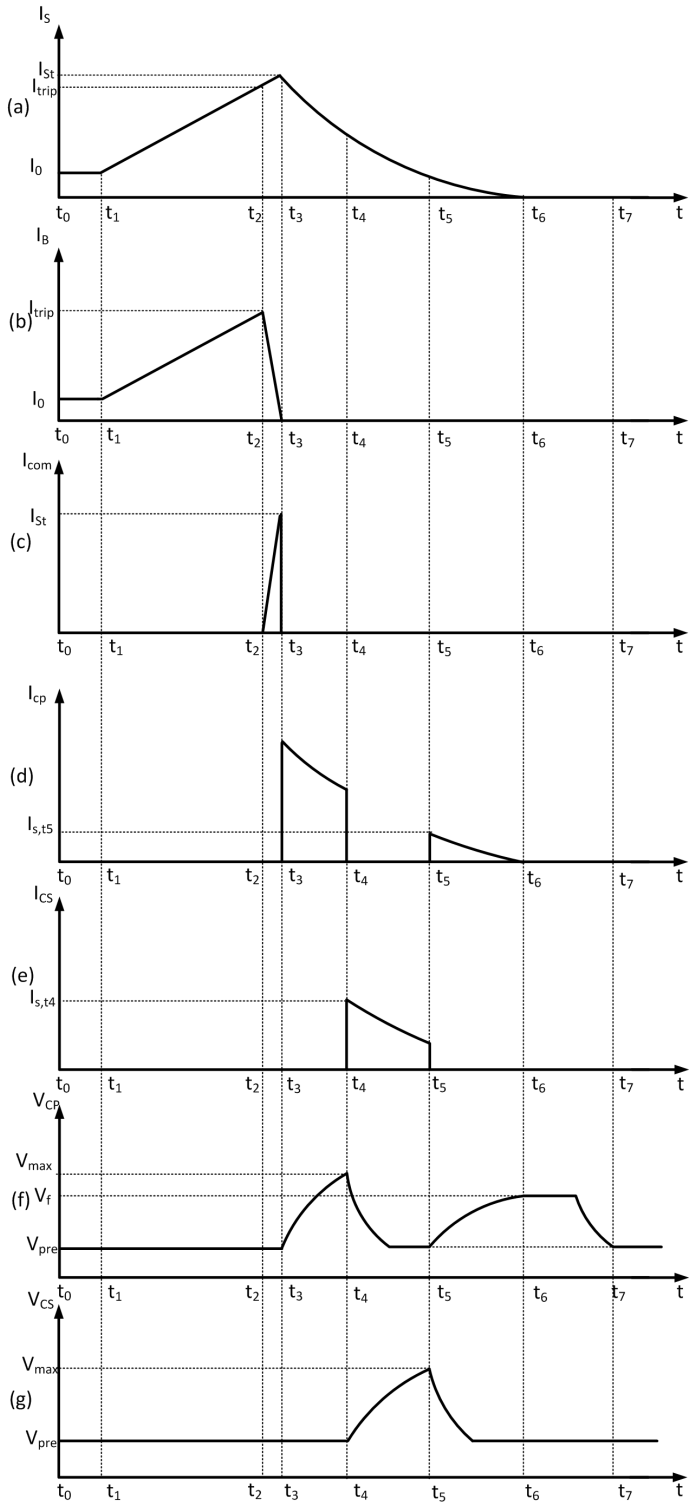

Figure 5.8: The interruption process of ACV DC-HCB, (a) line current (I_S), (b) current through the MCB (I_B), (c) main commutation current (I_{com}), (d) primary commutation current (I_{cp}), (e) secondary commutation current (I_{cs}), (f) primary commutation capacitor voltage (V_{cp}), and (g) secondary commutation capacitor voltage (V_{cs}).

Table 5.2

Parameter name	Parameters symbols
Source voltage	V_{DC}
System resistor & System inductor	R_T & L_T
Primary & Secondary Capacitor Voltage	V_{cp} & V_{cs}
Primary & Secondary Capacitance	C_{cp} & C_{cs}
the total commutation current	I_c
Line current	I_s
Current through the MCB	I_B

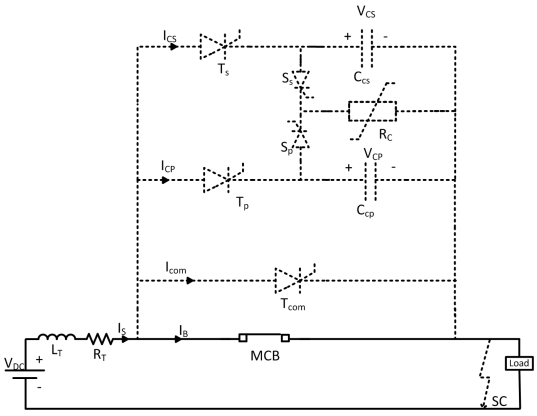

Figure 5.9: ACV DC-HCB circuit configuration during the first time interval

First Time Intervals ($t_0 < \mathbf{t} < t_1$)

Under the normal condition, the line current I_s, Fig 5.8 (a), is the rated current I_0, (5.2). The current through the MCB I_B, Fig 5.8 (b), is the same as I_B, and I_{com}, I_{cp} and I_{cs} are zero, Fig 5.8 (c) to Fig 5.8 (e). V_{cp}, Fig 5.8 (f), and V_{cs}, Fig 5.8 (g), are equal to V_{pre}.

Second Time Intervals ($t_1 < \mathbf{t} < t_2$)

The line current I_s reaches I_{trip} at the end of this interval. The line current I_s, Fig 5.8 (a), is given by (5.5), and I_B, Fig 5.8 (b), is the same as I_s. Other currents/voltages are the same as those of the previous interval as shown in Fig 5.8.

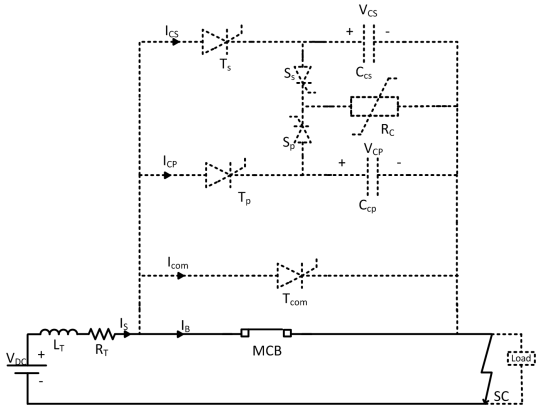

Figure 5.10: ACV DC-HCB circuit configuration during the secondary time interval

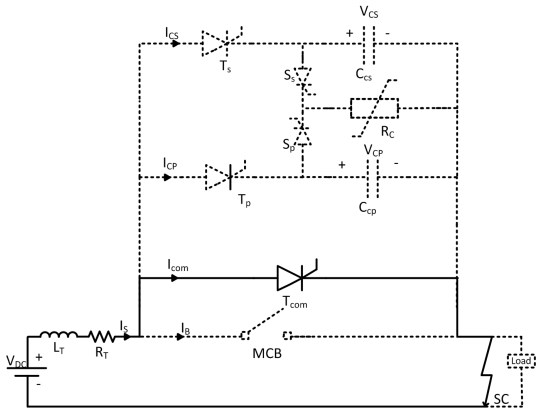

Figure 5.11: ACV DC-HCB circuit configuration during the third time interval

Third Time Intervals ($t_2 < \mathbf{t} < t_3$)

The interruption process starts in the third interval, and the operation time of the MCB is considered in this interval. At t_2, I_s reaches I_{trip} and the MCB opening is accompanied by turn-on of the main commutation switch T_{com}. Because of the DC arc, the line current I_s, Fig 5.8 (a) gradually flows into the main commutation path I_{com}, Fig 5.8 (c). At the end of the interval, the current through the MCB I_B, Fig 5.8 (b), becomes zero and the DC arc is extinguished. The length of this interval is equal to the operation time of the MCB, T_o, which is assumed to be 100 μs. It is assumed that I_c linearly increases and I_B linearly decreases. Since the maximum line current is I_{St}, I_{trip} is

$$I_{trip} = I_{St} - \frac{V_{DC}}{L_T} T_o. \tag{5.21}$$

During this time interval, I_{com} increases from 0 to I_{St} and I_B decreases from I_{trip} to zero. Therefore, the slope of I_{com} and I_B are

$$\frac{dI_{com}}{dt} = \frac{I_{St}}{T_o}, \tag{5.22}$$

$$\frac{dI_B}{dt} = -\frac{I_{trip}}{T_o}. \tag{5.23}$$

Since switches T_p and T_s did not operate, I_{cp} and I_{cs} are zero, and V_{cp} and V_{cs} are V_{pre} as given in Fig 5.8.

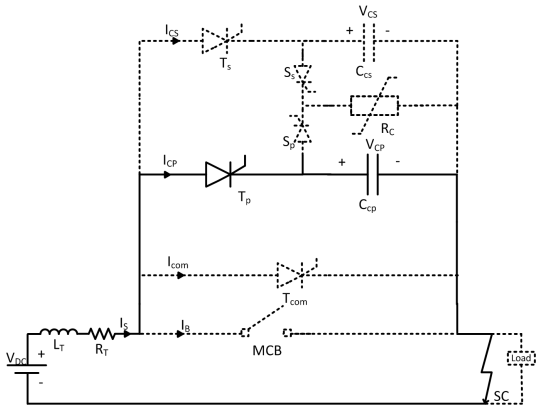

Figure 5.12: ACV DC-HCB circuit configuration during the fourth time interval

Fourth Time Intervals ($t_3 < \mathbf{t} < t_4$)

At the beginning of the fourth time interval, main commutation switch (T_{com}) turns off and the primary commutation switch (T_p) turns on at the same time as shown in Fig 5.12. I_{com}, Fig 5.8 (c), instantly drops to zero. The line current I_s, Fig 5.8 (a), flows into the primary commutation path and primary commutation current I_{cp}, Fig 5.8 (d), is I_s. The operation during this interval is similar to the third interval of the TCV DC-HCB. The system dynamics of this interval are given by

$$\begin{bmatrix} \dot{I_s}(t) \\ \dot{V_{cp}}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_T}{L_T} & \frac{1}{L_T} \\ \frac{1}{C_{cp}} & 0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_T} \\ 0 \end{bmatrix}, \tag{5.24}$$

$$\begin{bmatrix} I_{s0} \\ V_{cp0} \end{bmatrix} = \begin{bmatrix} I_{St} \\ V_{pre} \end{bmatrix}. \tag{5.25}$$

By solving (5.24) and (5.25), the capacitor voltage V_{cp} and the line current I_s are

$$V_{cp}(t) = V_{DC} + e^{-\alpha t}[(V_{pre} - V_{DC})cos(\beta_{cp}t) - \frac{1}{\beta_{cp}}(\alpha(V_{pre} - V_{DC}) + \frac{I_{St}}{C_{cp}})sin(\beta_{cp}t)], \tag{5.26}$$

$$I_s(t) = e^{-\alpha t}[I_{St}cos(\beta_{cp}t) - \frac{1}{\beta_{cp}}(\frac{V_{pre} - V_{DC}}{L_T} - \alpha I_{St})sin(\beta_{cp}t)], \tag{5.27}$$

where

$$\alpha = \frac{R_T}{2L_T}, \tag{5.28}$$

$$\omega_{cp} = \frac{1}{\sqrt{L_T C_{cp}}}, \tag{5.29}$$

$$\beta_{cp} = \sqrt{\omega_{cp}^2 - \alpha^2}. \tag{5.30}$$

At the end of this time interval, V_{cp}, Fig 5.8 (f), reaches V_{max} and the line current at t_4 is $I_{s,t4}$ which will be the initial condition of the next interval.

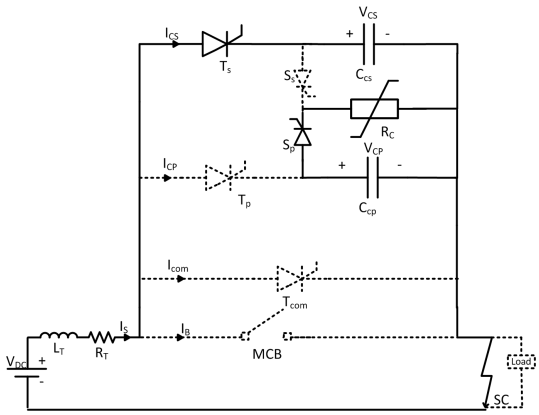

Figure 5.13: ACV DC-HCB circuit configuration during the fifth time interval

Fifth Time Intervals ($t_4 < \mathbf{t} < t_5$)

At the beginning of this interval, V_{cp} reaches V_{max} at t_4 and the secondary commutation switch T_s turns on. Because the voltage of the primary capacitor V_{cp} is larger than the

voltage of the secondary capacitor V_{cs}, the line current I_s, Fig 5.8 (a) flows into the secondary commutation path I_{cs}, Fig 5.8 (e), and thus the primary commutation switch T_p turns off, Fig 5.13. Therefore, I_{cp}, Fig 5.8 (d), is zero in this interval. After T_p turns off, the primary auxiliary switch S_p turns on and the primary commutation capacitor starts discharging the energy stored in the C_{cp}. The system of Fig 5.13 can be represented by Circuit A and Circuit B in Fig 5.14.

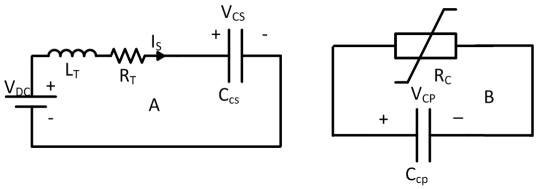

Figure 5.14: Representation of the system of Fig 5.13

When the voltage of the primary capacitor V_{cp}, Fig 5.8 (f), discharges to V_{pre}, S_p turns off and discharging process of Circuit B completes. At the end of the interval, the voltage of the secondary capacitor V_{cs}, Fig 5.8 (g), reaches V_{max}. The secondary capacitor voltage V_{cs} and the line current I_s of Circuit A satisfy

$$\begin{bmatrix} \dot{I_s}(t) \\ \dot{V_{cs}}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_T}{L_T} & \frac{1}{L_T} \\ \frac{1}{C_{cs}} & 0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_T} \\ 0 \end{bmatrix}, \tag{5.31}$$

$$\begin{bmatrix} I_{s0} \\ V_{cs0} \end{bmatrix} = \begin{bmatrix} I_{s,t4} \\ V_{pre} \end{bmatrix}. \tag{5.32}$$

The dynamics of Circuit B are governed by

$$C_{cp}\frac{dV_{cp}}{dt} + \frac{V_{cp}}{R_c} = 0. \tag{5.33}$$

Based on (5.31), (5.32) and (5.33), the line current I_s, the secondary capacitor voltage V_{cs} and the primary capacitor voltage V_{cp} are

$$V_{cs}(t) = V_{DC} + e^{-\alpha t}[(V_{pre} - V_{DC})cos(\beta_{cs}t) - \frac{1}{\beta_1}(\alpha(V_{pre} - V_{DC}) + \frac{I_{s,t4}}{C_{cs}})sin(\beta_{cs}t)], \tag{5.34}$$

$$I_s(t) = e^{-\alpha t}[I_{s,t4}cos(\beta_{cs}t) - \frac{1}{\beta_{cs}}(\frac{V_{pre} - V_{DC}}{L_T} - \alpha I_{s,t4})sin(\beta_{cs}t)], \tag{5.35}$$

$$V_{cp}(t) = V_{max}e^{-\frac{t}{\tau_{cp}}}, \tag{5.36}$$

where

$$\omega_{cs} = \frac{1}{\sqrt{L_T C_{cs}}}, \tag{5.37}$$

$$\beta_{cs} = \sqrt{\omega_{cs}^2 - \alpha_{cs}^2}, \tag{5.38}$$

$$\tau_{cp} = R_c C_{cp}. \tag{5.39}$$

During this process, the time for charging the secondary capacitor C_{cs} to the maximum voltage V_{max} should be longer than the discharging process of the primary capacitor C_{cp}. At the end of this interval, the line current drops to $I_{s,t5}$.

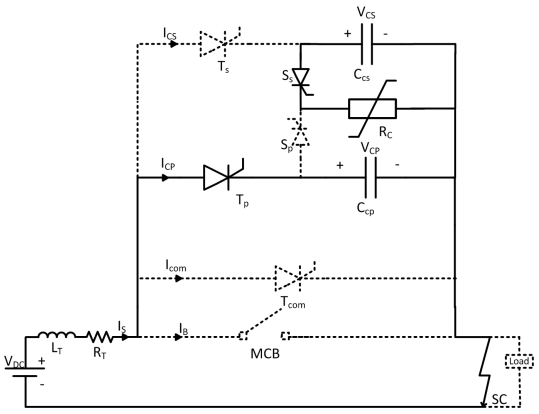

Figure 5.15: ACV DC-HCB circuit configuration during the sixth time interval

Sixth Time Intervals ($t_5 < \mathbf{t} < t_6$)

The sixth interval is similar to the fourth interval. The system of Fig 5.15 can be presented by Circuits C and D, Fig 5.16.

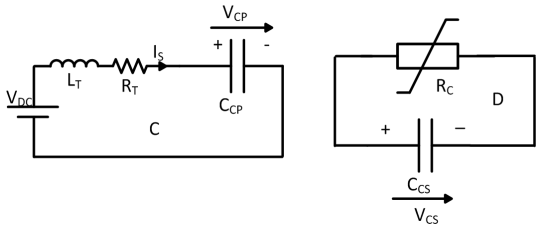

Figure 5.16: Representation of the system of Fig 5.15

Based on Circuit C, the line current I_s, Fig 5.8 (a), flows in the primary commutation path, i.e., I_{cp}, Fig 5.8 (d), with the initial value of $I_{s,t5}$. Hence, the secondary commutation current I_B, Fig 5.8 (b), remains zero in this interval. The dynamics of Circuit C are

$$\begin{bmatrix} \dot{I_s}(t) \\ \dot{V_{cp}}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_T}{L_T} & \frac{1}{L_T} \\ \frac{1}{C_{cp}} & 0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_T} \\ 0 \end{bmatrix}, \tag{5.40}$$

$$\begin{bmatrix} I_{s0} \\ V_{cp0} \end{bmatrix} = \begin{bmatrix} I_{s,t5} \\ V_{pre} \end{bmatrix}. \tag{5.41}$$

The secondary capacitor voltage V_{cs}, Fig 5.8 (g), of Circuit D, discharges from V_{max} to V_{pre} during this interval, based on

$$C_{cs}\frac{dV_{cs}}{dt} + \frac{V_{cs}}{R_c} = 0. \tag{5.42}$$

By solving (5.40), (5.41) and (5.42), the line current I_s, the primary capacitor voltage V_{cp} and the secondary capacitor voltage V_{cs} are

$$V_{cp}(t) = V_{DC} + e^{-\alpha t}[(V_{pre} - V_{DC})cos(\beta_{cp}t) - \frac{1}{\beta_1}(\alpha(V_{pre} - V_{DC}) + \frac{I_{s,t5}}{C_{cs}})sin(\beta_{cp}t)], \tag{5.43}$$

$$I_s(t) = e^{-\alpha t}[I_{s,t5}cos(\beta_{cp}t) - \frac{1}{\beta_{cp}}(\frac{V_{pre} - V_{DC}}{L_T} - \alpha I_{s,t5})sin(\beta_{cp}t)], \tag{5.44}$$

$$V_{cs}(t) = V_{max}e^{-\frac{t}{\tau_{cs}}}, \tag{5.45}$$

where

$$\tau_{cs} = R_c C_{cs}. \tag{5.46}$$

At the end interval, the line current I_s reaches to zero and the primary capacitor V_{cp} reaches to V_f which is normally less than V_{max} as shown in Fig 5.8 (f).

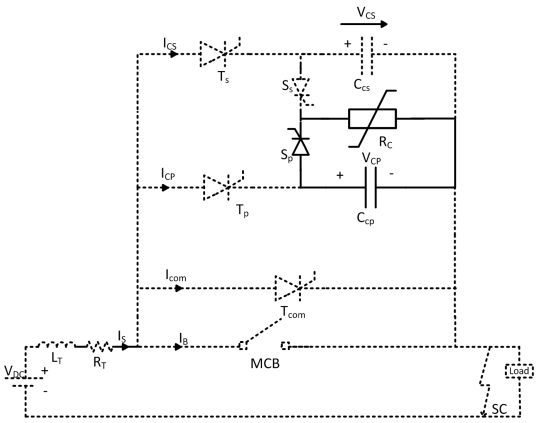

Figure 5.17: ACV DC-HCB circuit configuration during the seventh time interval

Seventh Time Intervals ($t_6 < \mathbf{t} < t_7$)

At the last time interval, the voltage of the primary capacitor V_{cp} discharges as shown in Fig 5.17 (f). Since the interruption process is finished, only the primary capacitor discharges in this interval, Fig 5.8. The interval ends when V_{cp} is equal to V_{pre}. The primary capacitor voltage V_{cp} is

$$V_{cp}(t) = V_f e^{-\frac{t}{\tau_{cp}}}. \tag{5.47}$$

In the case of Fig 5.8, it is assumed that Number of Switching (NoS) is three. The NoS is dependent on the total energy stored in the system inductor, the DC source voltage, and the commutation capacitances. In general, the total energy needed to be dissipated W_T is

$$W_T = \frac{1}{2} L_T I_{St}^2 + \int_{t_0}^{t_7} V_s I_s dt. \tag{5.48}$$

In (5.48), W_T depends on the energy stored in the system inductor and the energy needed to dissipated in the DC source during the interruption process. W_T can be also represented as

$$W_T = \frac{NoS-1}{4}(C_{cp}+C_{cs})(V_{max}^2 - V_{pre}^2) + \frac{1}{2}C_{cp}(V_{cpf}^2 - V_{pre}^2), \tag{5.49}$$

$$W_T = \frac{NoS}{4}C_{cp}(V_{max}^2 - V_{pre}^2) + \frac{NoS-1}{4}C_{cs}(V_{max}^2 - V_{pre}^2) + \frac{1}{2}C_{cs}(V_{csf}^2 - V_{pre}^2). \tag{5.50}$$

If NoS is an odd number, the last operating commutation switch is the primary commutation switch T_p. In this case, W_T can be represented by (5.49). In (5.49), V_{cpf} indicates the maximum voltage of the primary capacitor at the last time interval. Generally, V_{cpf} should be smaller than V_{max}. Equation (5.50) represents the case if the NoS is an even number. In (5.50), V_{csf} stands for the maximum voltage of the secondary capacitor at the last time interval which is always smaller than V_{max}. If both the primary commutation capacitor and secondary commutation capacitor have the same capacitance C_{com}. W_T is given as

$$W_T = \frac{NoS-1}{2}C_{com}(V_{max}^2 - V_{pre}^2) + \frac{1}{2}C_{com}(V_{cf}^2 - V_{pre}^2), \tag{5.51}$$

where V_{cf} indicates the maximum commutation capacitor voltage during last time interval.

5.3 Dynamic Performance of Counter-Voltage DC-HCBs

Last section discussed the interruption stages with the associated models of both counter-voltage DC-HCBs. In this section, we investigate the dynamic performance of both counter-voltage DC-HCBs. Based on the presented case studies, the TCV DC-HCB is compared with the proposed ACV DC-HCB.

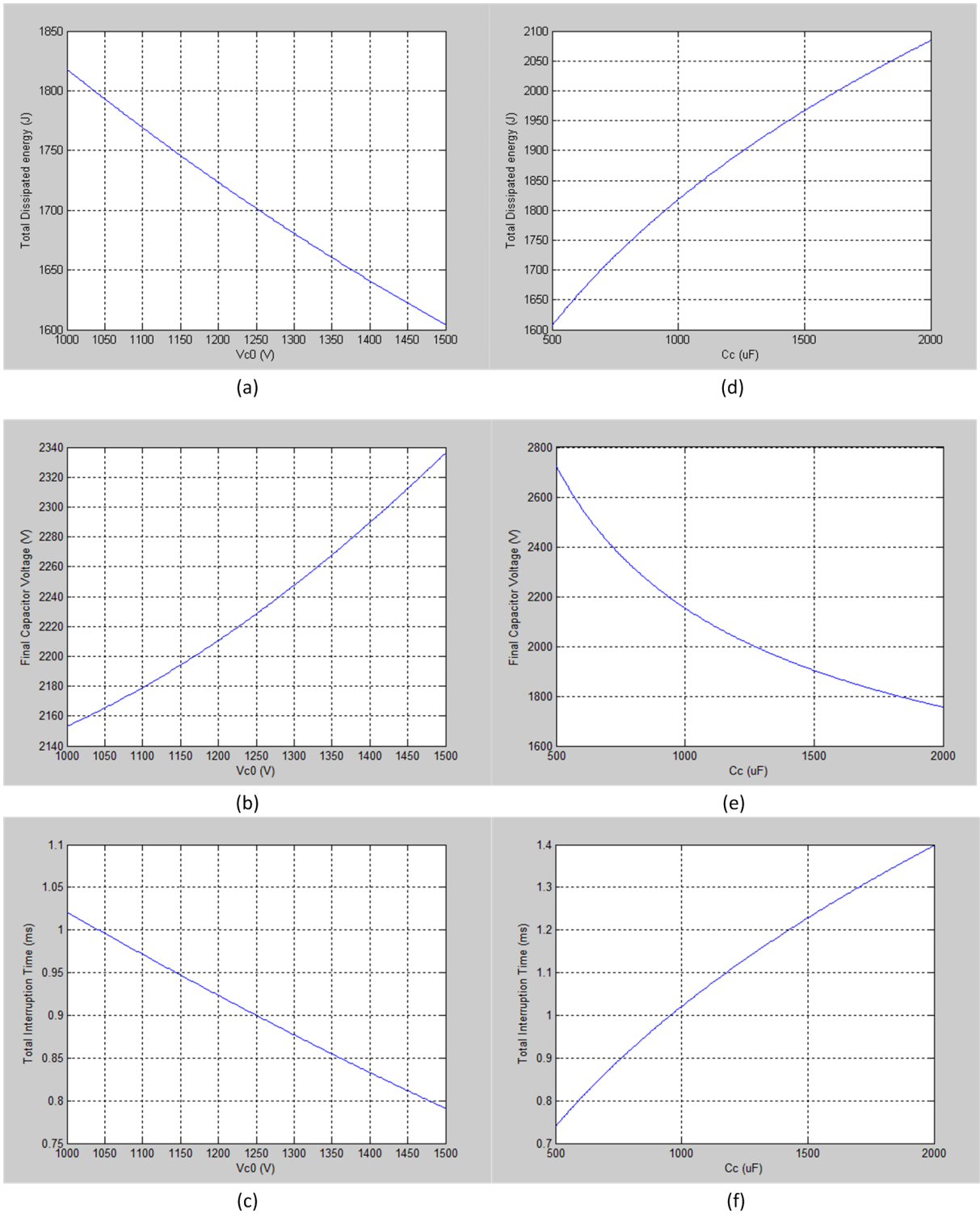

Figure 5.18: Effect of V_{pre} and C_c on the CB performance of TCV DC-HCB (Case A), (a) V_{pre} VS W_T, (b) V_{pre} VS V_{cf}, (c) V_{pre} VS TIT, (d)C_c VS W_T, (e)C_c VS V_{cf}, and (f)C_c VS TIT.

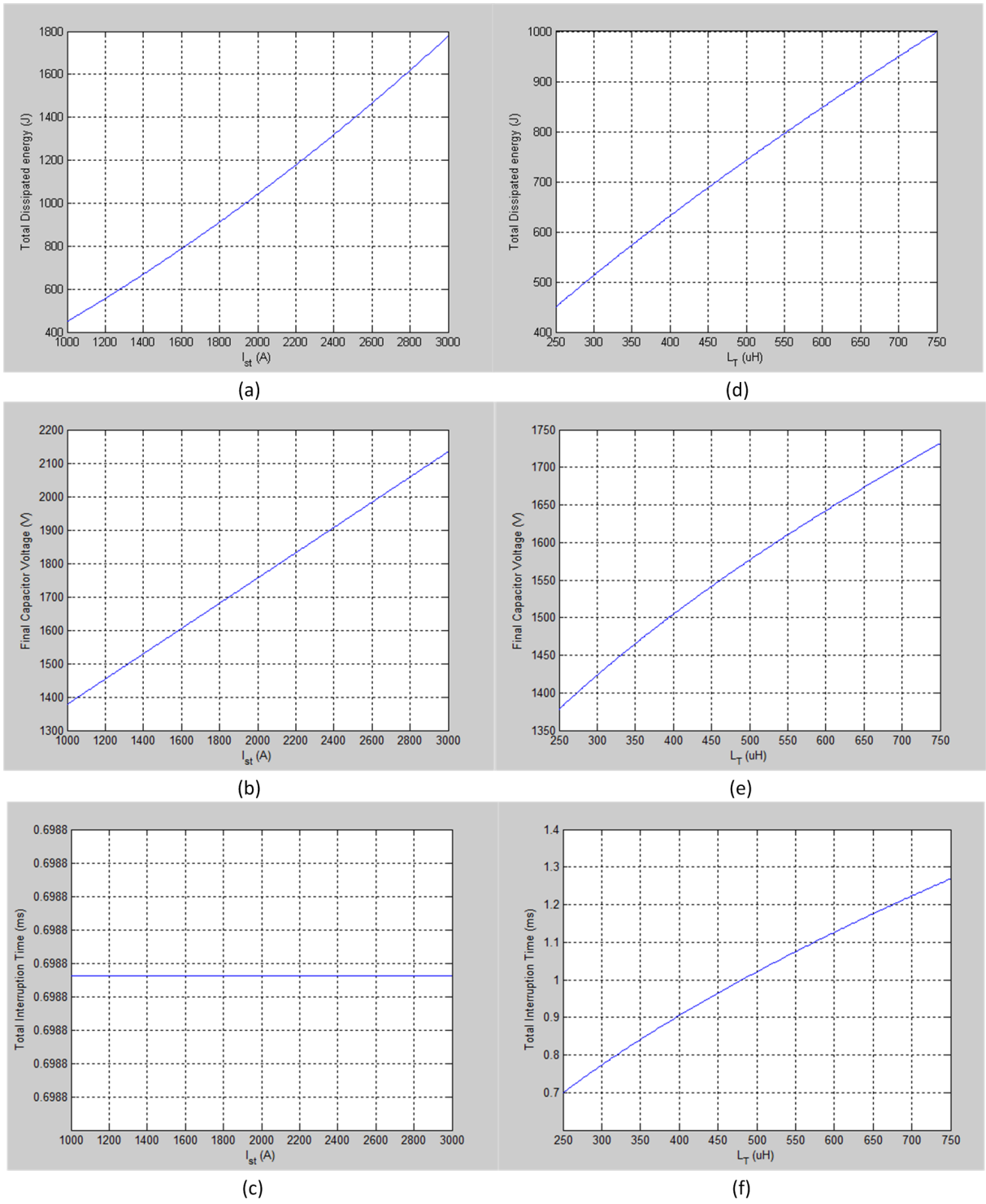

Figure 5.19: Effect of I_{St} and L_T on the CB performance of TCV DC-HCB (Case B), (a) I_{St} VS W_T, (b) I_{St} VS V_{cf}, (c) I_{St} VS TIT, (d)L_T VS W_T, (e)L_T VS V_{cf}, and (f)L_T VS TIT.

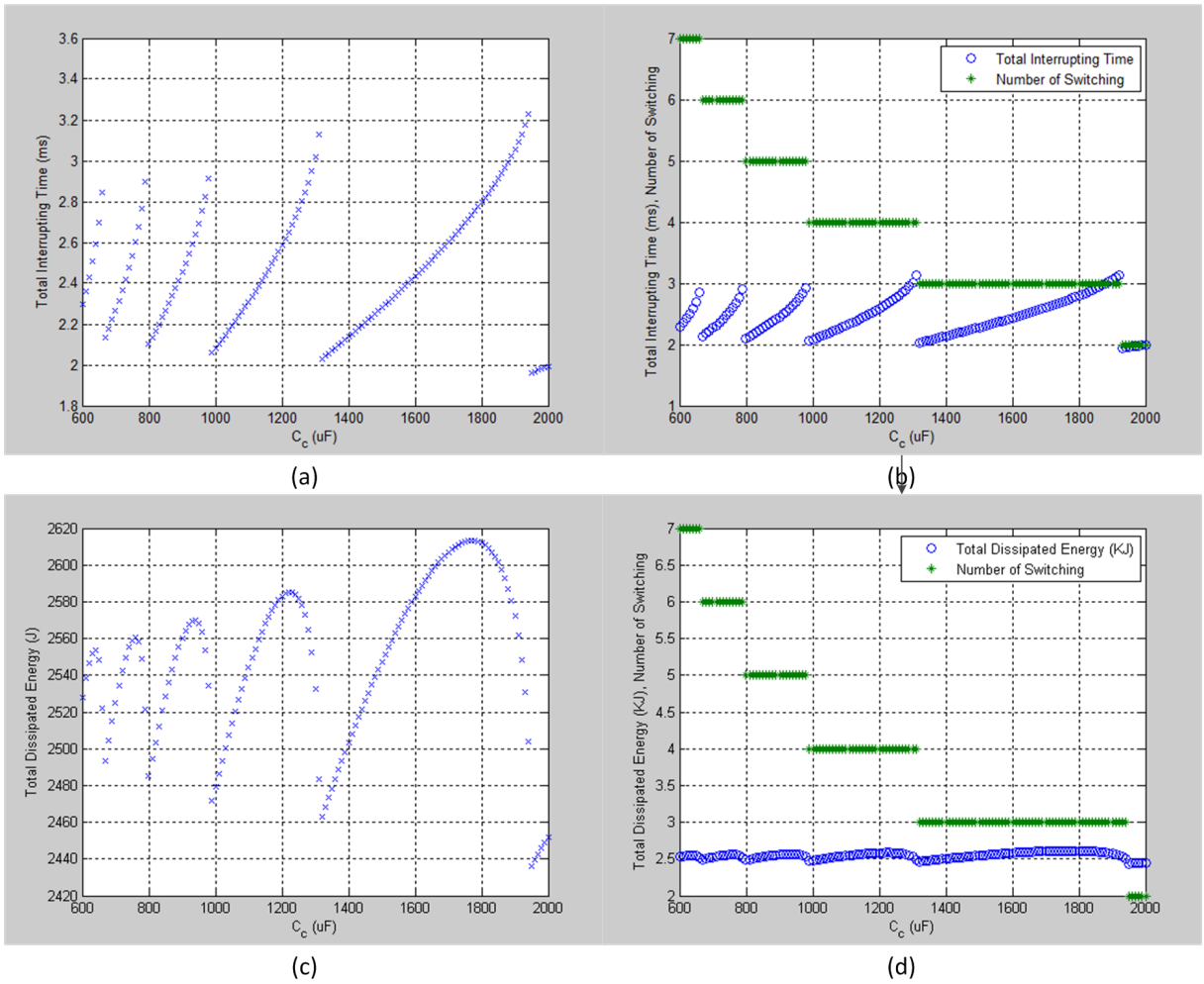

Figure 5.20: Effect of C_{com} on the CB performance of ACV DC-HCB (Case I), (a) C_{com} VS TIT, (b)C_{com} VS TIT with number of switching, (c) C_{com} VS W_T, and (d)C_{com} VS W_T with number of switching.

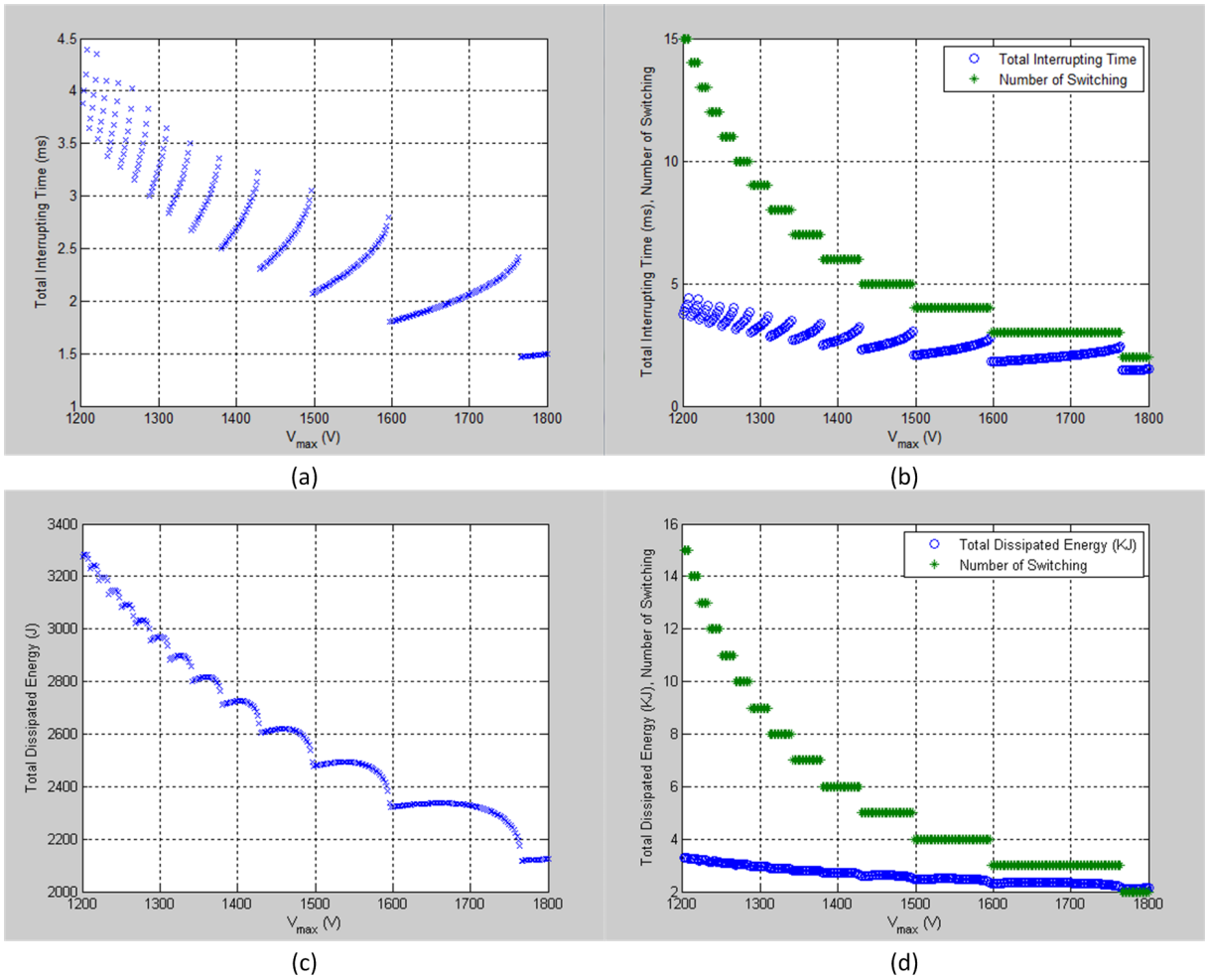

Figure 5.21: Effect of V_{max} on the CB performance of ACV DC-HCB (Case II), (a) V_{max} VS TIT, (b)V_{max} VS TIT with number of switching, (c) V_{max} VS W_T, and (d) V_{max} VS W_T with number of switching.

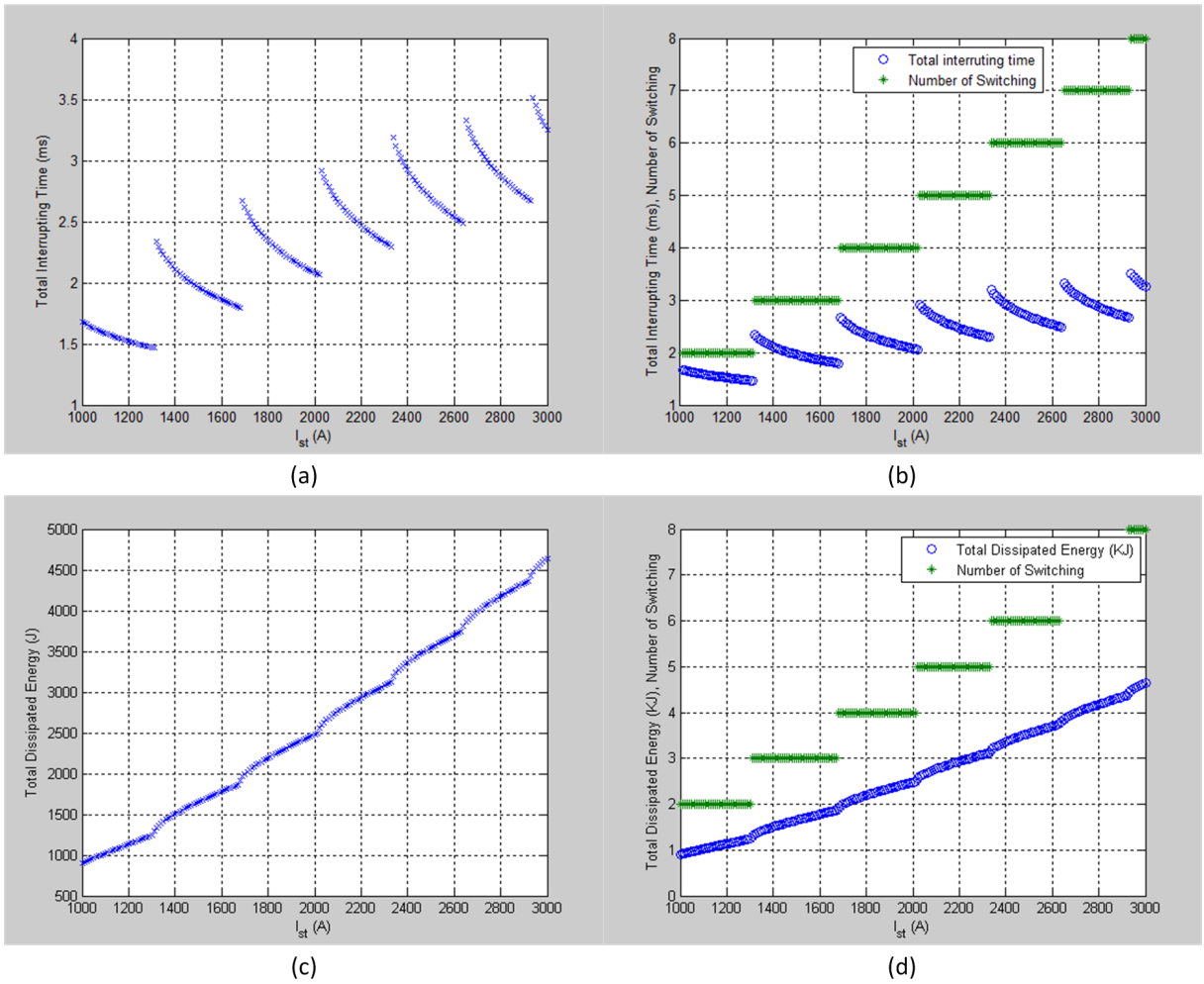

Figure 5.22: Effect of I_{St} on the CB performance of ACV DC-HCB (Case III), (a) I_{St} VS TIT, (b)I_{St} VS TIT with number of switching, (c) I_{St} VS W_T, and (d) I_{St} VS W_T with number of switching.

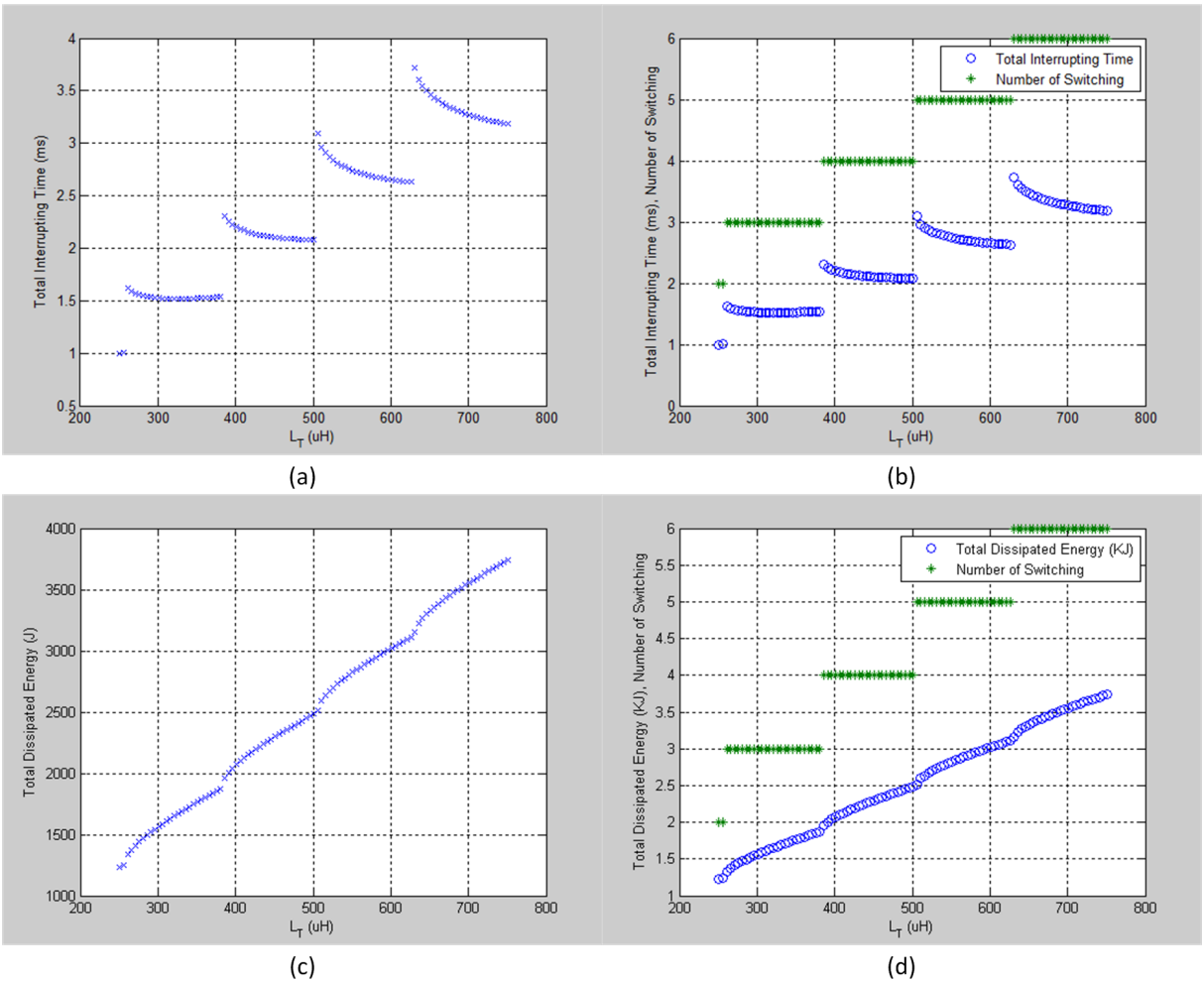

Figure 5.23: Effect of L_T on the CB performance of ACV DC-HCB (Case IV), (a) L_T VS TIT, (b)L_T VS TIT with number of switching, (c) L_T VS W_T, and (d) L_T VS W_T with number of switching.

5.3.1 Dynamic Performance of TCV DC-HCB

For the TCV DC-HCB, the commutation path only contains a capacitor and a diode., Hence, the only variables are the commutation capacitance (C_c) and the initial pre-charged voltage V_{pre}.

Case A, Fig 5.19, shows the effect of C_c and V_{pre} on the total interruption time (TIT), the final voltage of the capacitor V_f, and the total dissipated energy (W_T) by keeping other parameters constant. In Case A, the system inductor L_T and the trip current are 500 μH and 2000 A. Fig 5.19 (a) to Fig 5.19 (c) show the effect of V_{pre} when C_c is 1000 μF. Fig 5.19 (b) shows that higher values of V_{pre} result in higher values of the capacitor final voltage V_f. In contrast, higher values of V_{pre} lead to lower values of TIT and W_T

as shown in Fig 5.19 (a) and Fig 5.19 (c). Fig 5.19 (d) to Fig 5.19 (f) demonstrate the effect of C_c on the performance of TIT, V_f and W_T when V_{pre} is 1000V. Increasing the value of C_c results in decreasing of V_f, Fig 5.19 (e). Based on Fig 5.19 (d) and Fig 5.19 (f), the magnitudes of W_T and TIT increase when C_c increases.

Case B, Fig 5.19, shows the effect of I_{St} and L_T on the total interruption time (TIT), the final voltage of the capacitor V_f, and the total dissipated energy (W_T). In case B, the commutation capacitor C_c and the pre-charged voltage V_{pre} are 1000 μF and 1000 V. Fig 5.19 (a) to Fig 5.19 (c) examine the effect of I_{St} on the CB performances when L_T is 250 μH. Fig 5.19 (c) shows that TIT remains constant when I_{St} changes. This is because TIT is independent of I_{St} in (5.18). From Fig 5.19 (a) and Fig 5.19 (b), higher values of I_{St} lead to higher values of W_T and V_f. Fig 5.19 (d) to Fig 5.19 (f) focus on the dynamic performance of the TCV DC-HCB when L_T changes from 250 to 750 μH and I_{St} is 1000 A. From Fig 5.19 (d) to Fig 5.19 (f), the magnitudes of W_T, V_f and TIT all increase when L_T increases.

5.3.2 Dynamic Performance of ACV DC-HCB

For the ACV DC-HCB, it is assumed that both commutation capacitors are pre-charged to 1000V and have the same capacitance C_{com}. Different than the TCV DC-HCB, V_{max} is a variable parameter. Four different cases are considered in this section. They show the effects of C_{com}, V_{max}, L_T and I_{St} on the CB performance of TIT and W_T.

Case I, Fig 5.20, shows the effect of C_c on TIT and W_T. L_T and V_{max} are 500 μH and 1200V respectively, and the maximum current I_{St} is 2000A. From Fig 5.20 (a) and Fig 5.20 (b), higher values of C_c result in greater value of TIT with the same NoS. Fig 5.20 (c) and Fig 5.20 (d) depict that when C_{com} increases, W_T first increases and then decreases with the same NoS. From (5.51), W_T is determined by C_{com} and V_{cf}, and higher values of C_{com} lead to lower values of V_{cf}, if NoS remains unchanged. From Fig 5.20 (c), when C_{com} increase, W_T is first dominated by C_{com} which results in increasing of W_T, and then W_T is dominated by V_{cf} which decreases W_T.

Case II, Fig 5.21, demonstrates the dynamic performance of the ACV DC-HCB when V_{max} changed from 1200V to 1800V. In this Case, C_c, L_T and I_{St} are constants, at 1000 μF, 500 μH and 2000 A. Fig 5.21 (a) and (b) show that higher values of V_{max} lead to higher values of TIT with the same NoS. From Fig 5.21 (c) and (d), the value of W_T decreases as V_{max} increases.

Case III and Case IV, Fig 5.22 and Fig 5.23, show the dynamic performance of the

ACV DC-HCB for different values of I_{St} and L_T. For both cases, C_c and V_{max} remain unchanged. L_T is 500 μH for Case III and I_{St} is 2000 A for Case IV. Both cases exhibit similar dynamic performances. From Fig 5.22 (b) and Fig 5.23 (b), higher values of I_{St} or L_T lead to lower values of TIT with the same NoS. In contrast, higher values of I_{St} or L_T increase W_T in Fig 5.22 (d) and Fig 5.23 (d).

5.3.3 Discussion

Compared to the active mode DC-HCB and the ACV DC-HCB, the TCV DC-HCB has the simplest configuration without any commutation switch. However, the flexibility of the TCV DC-HCB is limited. The commutation capacitance is directly related to both TIT and W_T. The approach to reduce V_f of the TCV DC-HCB is to increase the commutation capacitor. Hence, it is not possible to achieve low C_c with low V_f.

With more flexibility, the ACV DC-HCB configuration is more complicated than that of the TCV DC-HCB. For the ACV DC-HCB, V_{max} is not dependent on C_{com}. From the dynamic performance of the ACV DC-HCB, V_{max} and C_{com} both determine the TIT and W_T, and V_{max} has a significant impact on the TIT and W_T. Large V_{max} results in fast interruption and low dissipated energy. Hence, the ACV DC-HCB can be designed based on low V_{max} and C_{com}. Therefore, the ACV DC-HCB is a preferred DC-HCB to TCV DC-HCB without considering the effect of DC arc.

5.4 Impact of DC arc

The previous section concluded that the proposed ACV DC-HCB is the preferred choice to the TCV DC-HCB. This section investigates the performances of both counter-voltage DC-HCBs based on using the PSCAD/EMTDC simulation platform while including the DC arc in the simulation model. One goal of the simulation studies is to demonstrate that the performances of both counter-voltage DC-HCBs, including the DC arc model are agreeable with the results presented in the previous section. Also, the simulation studies quantitatively demonstrates that the performance of the ACV DC-HCB is superior to that of the TCV DC-HCB, as well as the case where the MCB is opened directly without any commutation path. Finally, the simulation studies of ACV DC-HCB show that the minimum dielectric strength of the MCB is current dependent for the ACV DC-HCB.

For the simulations of both DC-HCBs, the DC study system is that of Chapter 3, Fig

3.10. For the TCV DC-HCB, only one case is considered. The system inductance L_T and the system resistance R_T are 500 μH and 0.2 Ω respectively. The maximum current I_{St} is 2000A. Three different commutation capacitances are selected and Table 5.3 summarizes all the results for the TCV DC-HCB. The first row is the results excluding the DC arc model while the last two rows demonstrate the simulation results including the arc model. By comparing the results of the first two rows, one concludes that the DC arc does not have a noticeable impact on the interruption behavior of the TCV DC-HCB.

Table 5.3: PSCAD/EMTDC simulation results of the TCV DC-HCB

C_c (μF)	$V_{cf}(V)$	K_{amin}	TIT (ms)
1000	2153.09	N/A	1.023
1000	2151.14	6350	1.031
14000	1200.61	5880	3.183

Table 5.4: PSCAD/EMTDC simulation results of the ACV DC-HCB

C_{com} (μF)	V_{max} (V)	K_{amin}	TIT (ms)	NoS	V_f (V)
Case i: I_{St} = 1000 A					
1000	1200	110.4	2.803	6	1142.6
Case ii: I_{St} = 2000 A					
3300	1200	N/A	4.177	5	1121.6
2200	1200	162.1	3.912	7	1157.03
3300	1200	160.4	4.288	5	1097.71
Case iii: I_{St} = 4000 A					
3300	1500	220.4	4.125	4	1243.4

Table 5.4 summarizes all the results for the ACV DC-HCB. Three cases are considered for the ACV DC-HCB. The propose of introducing three cases is to demonstrate that the minimum dielectric strength of contact gap K_{amin} for the ACV DC-HCB is current dependent. Hence, three different maximum line currents (I_{St}) are selected, which are 1000A, 2000A, and 4000A. The system inductance L_T and the system resistance R_T are 500 μH and 0.2 Ω. Based on these three cases, higher values of I_{St} results in higher values of $K_{a,min}$.

The first row of Case ii, Table 5.4, is the result excluding the DC arc model and the secondary row of Case ii is the simulation result including the DC arc model. By comparing the results of these two rows, the total interruption time (TIT) including the DC

arc model is slightly larger than the TIT without including the DC arc model. Therefore, one can conclude that the DC arc does not noticeable impact on the interruption performance of the ACV DC-HCB.

The results of Case ii of Table 5.4 is also used to compare with that of the TCV DC-HCB to quantitatively show that the performance of the ACV DC-HCB is superior to that of the TCV DC-HCB. From Table 5.3, to interrupting the fault current at 2000A, the TCV DC-HCB requires C_c to be 14000 μF, if the maximum blocking voltage of SSCB is about 1200V. This is not a practical approach by using such large capacitances. In contrast, the ACV DC-HCB can set V_{max} to be 1200V with different combination of the capacitors, Case ii of Table 5.4. Each commutation capacitor can be selected as a capacitor implemented by one single bank, which reduces the weight and size. Moreover, K_{amin} of the ACV DC-HCB is much less than K_{amin} of the TCV DC-HCB. Therefore, we conclude that the proposed ACV DC-HCB is superior to the TCV DC-HCB.

Finally, we compare the proposed ACV DC-HCB with the DC-CB without the commutation path in Chapter Three. From Table 3.4 of Chapter three, the DC-CB without the commutation circuit requires K_{amin} to be 3645.2. Moreover, the DC-CB without the commutation circuit results in large over-voltage across the inductor and long arcing time. In contrast, the proposed ACV DC-HCB only need K_{amin} to be 162.1, Table 5.4. Furthermore, most of the energy is absorbed by the commutation capacitors and the acing time is short compared to that of the DC-CB without the commutation circuit. Therefore, the proposed ACV DC-HCB is superior to the DC-CB without the commutation circuit as well.

5.5 Conclusion

In this Chapter, two counter-voltage DC-HCBs, i.e., TCV DC-HCB and ACV DC-HCB, were introduced. First, we described interruption process of the two counter-voltage DC-HCBs without considering the DC arc. Based on the analysis, interruption stages and the associated models of both DC-HCBs were discussed. Then the dynamic performance of both DC-HCBs were investigated. By comparing the dynamics performance of two DC-HCBs, we concluded that the performance of the proposed ACV DC-HCB is superior to that of the TCV DC-HCB, without considering the DC arc. The reason is that the ACV DC-HCB can operate based on low V_{max} and C_{com} whereas the TCV DC-HCB cannot. Section 5.4 presented the simulation studies on both counter-voltage DC-HCBs considering the DC arc model, using PSCAD/EMTDC simulation software. From the

simulation results, we demonstrated that the DC are does not have a noticeable impact on the interruption performance for both DC-HCBs. we also concluded that the ACV DC-HCB is a preferred choice to the TCV DC-HCB. The advantages of the ACV DC-HCB are: i) K_{amin} of ACV DC-HCB is much lower than that of TCV DC-HCB, and ii) Commutation capacitance C_{com} of ACV DC-HCB is much lower than that of the TCV DC-HCB. The studies also demonstrate that the ACV DC-HCB is the preferred choice to the DC-CB, without the commutation path. In the next chapter, the proposed ACV DC-HCB performance is compared with the active mode DC-HCB of the FCZ interruption.

Chapter 6

Performance Evaluation of the Proposed DC-HCB

6.1 Introduction

Chapter 4 concludes that active mode DC-HCB, based on the first current-zero (FCZ) interruption, provides a superior performance to that of the second current-zero (SCZ) interruption. Chapter 5 concludes that the proposed alternative counter-voltage (ACV) DC-HCB is a preferred choice to the traditional counter-voltage (TCV) DC-HCB. In this Chapter, the first goal is to compare the active mode DC-HCB based on the FCZ interruption with the proposed ACV DC-HCB. From the comparison, the proposed ACV DC-HCB is identified as the preferred option. The next objective is to select the commutation circuit parameters of the ACV DC-HCB to interrupt a 5 kA DC fault within 5 ms with the system voltage of up to 1 kV. Finally, we evaluate the performance of the proposed ACV DC-HCB in the study system introduced in Chapter 2.

6.2 Comparison of Active Mode DC-HCB with ACV DC-HCB

In this section, the active mode DC-HCB based on the FCZ interruption is quantitatively compared with the ACV DC-HCB. The propose of the comparison is to demonstrate that the interruption performance of the ACV DC-HCB is superior to that of the active mode DC-HCB.

The DC study system for the DC-HCB comparison is the same as that of Chapter 3, Fig 3.10. The System inductor L_T and the system resistor R_T are 500 μH and 0.2 Ω repetitively. The configuration of the active mode DC-HCB is shown in Fig 6.1 which is the same as that of the active mode DC-HCB in Chapter 4, Fig 4.1. When the line current I_s, Fig 6.1, reaches 2000 A, S_c, turns on and the interruption process starts. The frequency of the commutation LC circuit ω_1, (4.12), is 1000 Hz. The configuration of the ACV DC-HCB, Fig 6.2, is also the same as that of ACV DC-HCB in Chapter 5, Fig 5.7. When the line current reaches 2000 A, the primary commutation switch T_p turns on. Hence, the main commutation switch T_{com}, Fig 6.2, turns on at 1800 A based on (5.21). For the ACV DC-HCB, the maximum line current is always 2000 A. The pre-charged voltage of both commutation capacitors are 1000 V which is the same as the source voltage V_{DC}, Fig 6.2. Table 6.1 and Table 6.2 summarize the PSCAD-based simulation results of both active mode DC-HCB and the ACV DC-HCB respectively.

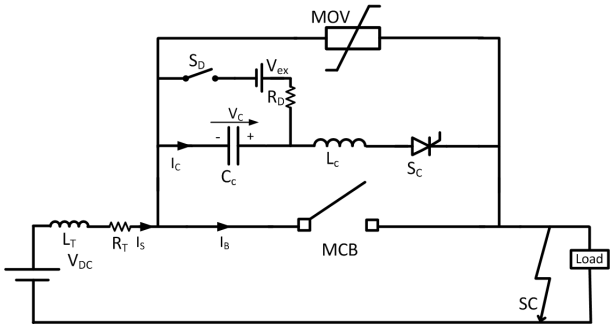

Figure 6.1: Circuit configuration of active mode DC-HCB

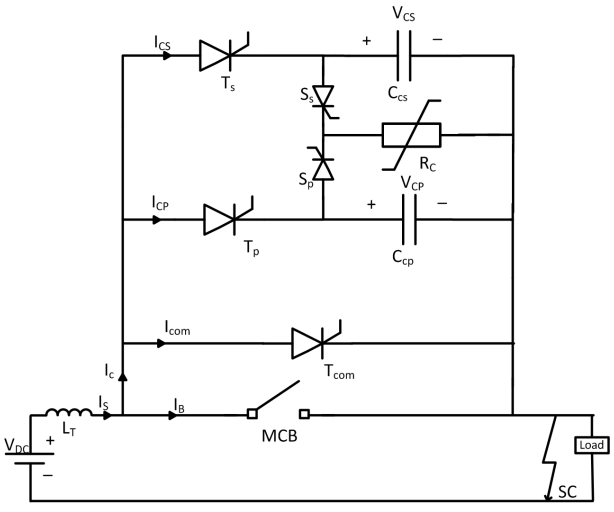

Figure 6.2: Circuit configuration of Alternative Counter-voltage(ACV) DC-HCB

In our simulation studies, the values of V_{max} (maximum blocking voltage of the switches), 1200 and 1500 V, are selected. When V_{max} is 1200, only the proposed ACV DC-HCB can interrupt the fault current within 5 ms. When V_{max} is 1500 V, both DC-HCB can interrupt the fault current within 5 ms. For the active mode DC-HCB, there is no direct control on V_{max}. Therefore, V_{max} is controlled based on the values of the commutation capacitor C_c and the pre-charged capacitor voltage V_{pre}.

There are three cases in Table 6.1. The first two cases summarize the simulation results when V_{max} is 1500 V. The dielectric strength of the gap K_a is selected as the minimum dielectric strength K_{amin} for Case I. In Case II, K_a is larger than K_{amin}. The total interruption time (TIT) of Case II is slightly greater than that of Case I. However, the maximum current I_{max} of Case II is much lower than that of Case I. Based on Table 4.2 in Chapter Four, we had the same observation. Although K_{amin} of the active mode DC-HCB, based on the FCZ interruption, is low, it is not practical to select K_a to be K_{amin}. Generally, a large value of K_a is required to reduce I_{max}. Case III of Table 6.1 shows the simulation results when V_{max} is 1200 V. In this case, a large capacitance C_c, 12000 μF, is chosen. The TIT is much longer than 5 ms which does not meet the interruption time requirement. Hence, Case III, with V_{max} of 1200 V, is not a practical option for the active mode DC-HCB.

Table 6.1: PSCAD-based simulation results of the active mode DC-HCB

Case	C_c (μF)	V_{max} (V)	K_a	V_{pre} (V)	TIT (ms)	I_{max}
I	4800	1494.3	176.3	150	4.293	3536.3
II	4800	1494.4	900	150	4.442	2803.5
III	12000	1199.1	900	100	7.893	3223.3

In the simulation studies of the ACV DC-HCB, Table 6.2, both the primary capacitor C_{cp} and the secondary capacitor C_{cs} of Fig 6.2 are selected to be C_{com}, and both commutation capacitor are pre-charged to be the same voltage V_{pre}. The maximum blocking voltage V_{max} of the ACV DC-HCB is a variable parameter. Hence, V_{max} is not dependent on the pre-charged capacitor voltage V_{pre} and the commutation capacitance C_{com}. Two different cases are simulated for the ACV DC-HCB and summarized in Table 6.2. Since V_{max} is not dependent on C_{com}, C_{com} can be theoretically any acceptable value. The dielectric strength of contact gaps K_a is selected as K_{min} for both cases.

Table 6.2: PSCAD/EMTDC simulation results of the ACV DC-HCB

Case	C_{com} (μF)	V_{max} (V)	K_{amin}	TIT (ms)	NoS
A	1000	1500	163.4	2.122	4
B	3300	1200	157.3	4.288	5

From the comparison of Table 6.1 and Table 6.2, we conclude that conclude that the ACV DC-HCB has the superior performance than the active mode DC-HCB. By comparing Case A of Table 6.2 with Case I and Case II of Table 6.1, the active mode DC-HCB requires larger capacitance than that of the ACV DC-HCB, and the TIT of active mode DC-HCB is longer than that of the ACV DC-HCB. Furthermore, I_{max} of the active mode DC-HCB is much higher than that of the ACV DC-HCB. For Case B of Table 6.2, V_{max} is 1200 V and the TIT is 4.136 ms, which is less than 5 ms. However, when V_{max} of the active mode DC-HCB is 1200V, Case III of Table 6.1, the TIT is longer than 5 ms. Last, K_a required for ACV DC-HCB is lower than that of the active mode DC-HCB. In a conclusion, the advantages of the ACV DC-HCB compared to the active mode DC-HCB are: i) lower V_{max} and I_{max}, ii) smaller capacitance of C_{com}, and iii) lower K_a.

6.3 Performance of the ACV DC-HCB in the DC Study System

From the previous section, we conclude that the ACV-HCB is the preferred option to the active mode DC-HCB. In this section, we present a ACV DC-HCB that can interrupt the fault current up to 5 kA in 5 ms with the system voltage of up to 1 kV. This section demonstrates the procedures to select the commutation parameters of the ACV DC-HCB and shows that the ACV DC-HCB is capable of interrupting different values of fault current (up to 5000 A) even when the system inductor is larger (500 μH). The DC study system is the same as Chapter 3, Fig 3.10. The system inductance L_T and resistance R_T are 500 μH and 0.2 Ω. Under this circumstance, the maximum fault current is 5000A based on (5.7). The configurations of the ACV DC-HCB is the same as given by Fig 6.2.

From the dynamic performance of the ACV DC-HCB in Chapter 5, V_{max} and C_{com} are the parameters that impact the total interruption time (TIT) of the ACV DC-HCB. V_{max} has a greater effect on TIT as compared with that of C_{com}. To reduce the size and weight, the commutation capacitors are selected as the capacitor that can be implemented by one

single bank. Generally, V_{max} should be as low as possible, but a lower value of V_{max} might result in a higher value of TIT. Therefore, the first objective is to select the lowest V_{max} that TIT can be within 5 ms. This process uses the mathematical model of the ACV DC-HCB without considering the DC arc model. Table 6.3 summarizes the analytical results corresponding to the case that TIT can be within 5 ms when the maximum fault current I_{St} is 5000 A.

Table 6.3: Analytical results of the ACV DC-HCB (1)

Case	V_{max} (V)	C_{com} (μF)	TIT (ms)
1	1400	2200	4.092
2	1400	1500	4.807
3	1500	2200	3.901
4	1500	1500	3.810
5	1550	1500	3.770
6	1550	2200	3.552

V_{max} increases from 1200 V to 1550 V in steps at either 50 or 100 V. When V_{max} is either 1200 or 1300 V, the TIT is greater than 5 ms. Therefore, Table 6.3 lists the results for V_{max} at 1400 V and above. From the dynamic performance of the ACV DC-HCB in Chapter Five, lower values of the maximum current I_{St} might results in higher value of TIT, Fig 5.22. Therefore, the next step is to verify the cases in Table 6.3, if the fault current interruption, up to 5000 A, within 5 ms can be achieved.

Table 6.4: Analytical results of the ACV DC-HCB (2)

Case	V_{max} (V)	C_{com} (μF)	TIT (ms)	I_{St} (A)
1	1400	2200	5.194	4580
2	1400	1500	5.255	4920
3	1500	2200	4.913	4610
4	1500	1500	4.895	4670
5	1550	1500	4.528	4720
6	1550	2200	4.444	4455

From Table 6.4, Case 1 and Case 2 do not meet the requirement since the TIT is over 5 ms. In Table 5.4 of Chapter Five, the TIT obtained from the PSCAD/EMTDC simulation

results is slightly longer than that of results without considering the DC arc model in the studies. Hence, the next procedure is to simulate Case 3 to Case 6 of Table 6.4 in the PSCAD/EMTDC to identify if the TITs of these four cases can be within 5 ms. The simulation results are listed in Table 6.5.

Table 6.5: PSCAD simulation results of the ACV DC-HCB (1)

Case	V_{max} (V)	C_{com} (μF)	TIT (ms)	I_{St} (A)
3	1500	2200	5.112	4612
4	1500	1500	5.095	4672
5	1550	1500	4.772	4721
6	1550	2200	4.721	4450

From the simulation studies, Table 6.5, only TITs of Case 5 and Case 6 are within 5 ms. The last step is to consider the switching delay of the SSCB. One of the SSCBs meets our voltage and current range is the MITSUBISHI HV-IGBT model, CM2400HC-34N. The total turn-on and turn-off delay of the SSCB (T_{delay}) are 4.5 μs. From Fig 5.8 of Chapter Five, the interruption process starts at the fourth interval. C_{cp} is charged in the fourth interval and discharged at the fifth interval. The discharged process of C_{cp} requires to turn on and turn off S_p, Fig 5.7. Hence, the fifth interval T_{fif} should be longer than the sum of discharging time of C_{cp} and T_{delay}. Based on (5.36), the discharging time of the primary capacitor T_{pd} can be given as

$$T_{pd} = R_c C_{cp} ln(\frac{V_{max}}{V_{pre}}), \tag{6.1}$$

where

$$R_c = \frac{V_{max}}{I_{St}}. \tag{6.2}$$

By choosing this value of R_c, the maximum discharging current will be the same as the maximum line current I_{St}. The total discharging time T_d is

$$T_d = T_{dealy} + T_{pd}. \tag{6.3}$$

Table 6.6: PSCAD simulation results of the ACV DC-HCB (2)

Case	V_{max} (V)	C_{com} (μF)	T_{fif} (ms)	T_d (ms)
5	1550	1500	0.2031	0.2142
6	1550	2200	0.3226	0.3133

Table 6.6 lists the simulation results of Case 5 and Case 6 when the maximum line current I_{St} is 5000A. From the results, only T_{fif} of Case 6 is longer than T_d. Therefore, Case 6 is our final selection. In this case, the ACV DC-HCB can interrupt the fault current up to 5 kA within 5 ms for the system voltage of up to 1 kV. From the studies, we conclude that the ACV DC-HCB can perform the proper fault interruption under large system inductance (500 μH) with different current levels.

6.4 Performance Evaluation of the ACV DC-HCB

From the pervious part, we first concluded that the ACV DC-HCB has a superior performance to that of the active mode DC-HCB. Then, a ACV DC-HCB is selected to successfully interrupt the fault current of up to 5 kA in 5 ms with the DC source voltage of up to 1 kV when the system inductor is relatively large. In this section, our objective is to evaluate the performance of the ACV DC-HCB in the LVDC study system introduced in Chapter 2. The simulation studies of this section focus on investigating the performance of ACV DC-HCB when different system inductances L_T are considered.

6.4.1 LVDC Study System

The DC study power system is the low-voltage direct current (LVDC) distribution system, Fig 6.3 [13]. The LCC is a rectifier, Part B of Fig 6.3, and operates to control the DC line current to its reference value. The VSC at the inverter side, Part A of Fig 6.3, operates to control the DC line voltage. The ACV DC-HCB is located at the VSC side of the DC link.

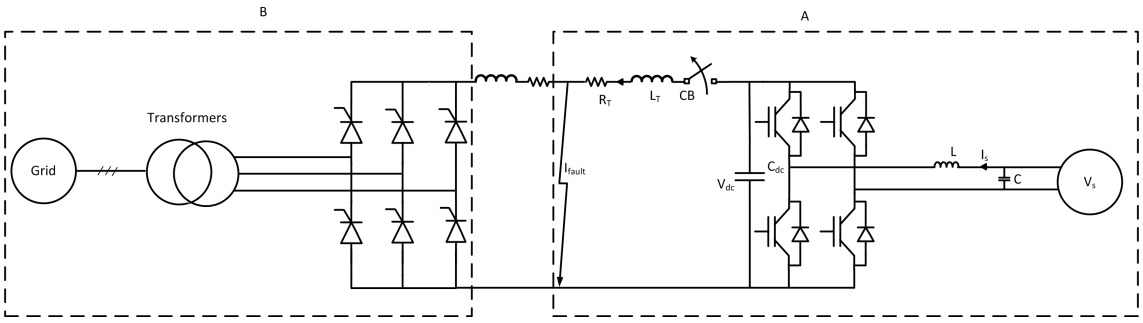

Figure 6.3: Configuration of the LVDC distribution network

Table 6.7: System Parameters of the LVDC study system model

System Parameter	Value
V_{dc}	750 V
C_{dc}	3.5 mF
L_c	250 μH/km
R_c	0.1 Ω/km
V_s	120 V
L	430 μH
C	8 μF

In Table 6.7, V_{dc} is the DC line current of the power system, and the C_c indicates the DC capacitance, I_{dc} is the DC line current, L_c and R_c are the DC cable inductance per kilometer and the DC cable resistance per kilometer. It is assumed that the maximum cable length is 2 km. Based on Table 6.7, the effective DC inductance L_T can be as large as 500 μH and the maximum value of R_T is 0.2 Ω.

6.4.2 Performance Evaluation

In this section, performance evaluation of the ACV DC-HCB, Fig 6.4, implemented in the DC study system, is presented when the fault is applied at different locations of the DC line. The diode bridge is used in the ACV DC-HCB. The circuit parameters of the DC-HCB are shown in Table 6.8.

During the fault, a RLC circuit is formed as shown in Fig 6.5. C_{dc} of the Fig 6.3 rapidly discharges and the maximum fault current depends on R_T, C_{dc} and L_T. Based on the C_{dc} selected in Table 6.7, the ACV DC-HCB is to interrupt a 1000A fault current when

the effective line inductance L_T is 500 μH. Hence, I_{trip}, which is the line current when the MCB opens, is

$$I_{trip} = 1000 - \frac{V_{dc}}{L_T}T = 1000 - \frac{750}{500 \times 10^{-6}}100 \times 10^{-6} = 875A, \tag{6.4}$$

where T stands for the operation time of the MCB which is 100 μs. In (6.4), it is considered that V_{dc} is constant during the fault interruption. In this section, it is considered that I_{trip} is 875 A regardless of the fault location. Therefore, I_{max} is dependent on the effective line inductance L_T and the DC line voltage V_{dc} as

$$I_{max} = I_{trip} + \frac{V_{dc}}{L_T}T. \tag{6.5}$$

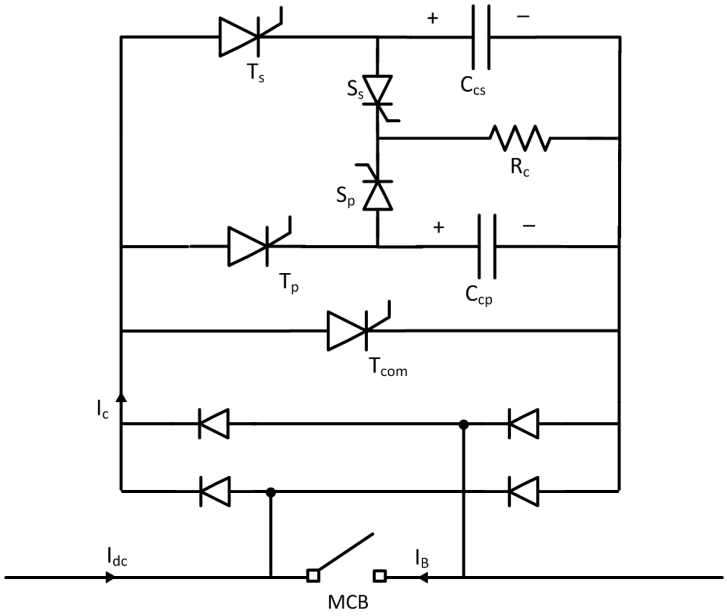

Figure 6.4: The configuration of the ACV DC-HCB implemented in LVDC study system model

The circuit parameters of the ACV DC-HCB are listed in Table 6.8. Same as Chapter 5, the value of the primary capacitance C_{cp}, Fig 6.4, and the secondary capacitor C_{cs}, Fig 6.4, are the same, and the maximum voltage V_{max} of both the commutation capacitors is 1.2 times of the system voltage V_{dc}.

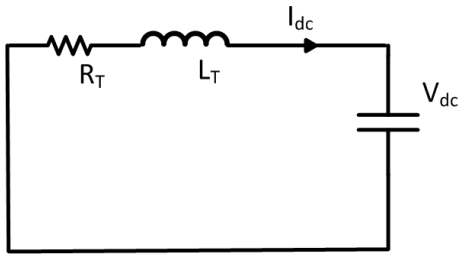

Figure 6.5: Representation Part A of the Fig 6.3 when a fault is applied

Table 6.8: Circuit Parameters of the ACV DC-HCB in LVDC study system model

System Parameter	Value
V_{pre}	750 V
C_{cp}	680 μF
C_{cs}	680 μF
V_{max}	900 V
I_{trip}	875 A

Since the objective is to evaluate the ACV DC-HCB performance when the fault is applied at different locations of the DC line, three different cases with different fault locations are considered. Our requirements for the ACV DC-HCB in this section are i) the total interruption time (TIT) should be less than 5 ms, and ii) the maximum line current I_{max} should be less than 1200 A. From (6.5), lower values of L_T results in high values of I_{max}. Therefore, the second requirement is to limit I_{max} to protect the components in the circuit, i.e., SSCBs.

In Case I, the fault is applied to DC line at the rectifier side. Hence, the effective L_T is at its maximum value which is 500 μH. The simulation waveforms of the Case I is shown in Fig 6.6. The fault is applied at 0.15 s. The MCB starts to open when I_B, Fig 6.6 (a) reaches I_{trip}, and accompanied with turning on T_{com}, Fig 6.4. I_{dc}, Fig 6.6 (e) increases gradually, depending on the V_{dc} and L_T. After about 100 μs, I_{dc} totally flows into the commutation path I_c, Fig 6.6 (c). At the same time, the DC arc is extinguished and the commutation capacitors begin to absorb the system energy. From Fig 6.6 (b) and Fig 6.6 (d), the total number of switching events (NoS) is 7 in Case I. During the fault, V_{dc} decreases, as shown in Fig 6.6 (f). The interruption time in this case is 1.1663 ms and the maximum line current I_{max} is 980.3A. From Fig 6.6, the performance of ACV DC-HCB in Case I fulfills our requirement.

In case II, Fig 6.7, the DC fault is applied at the middle of the DC line at 0.15 s . Hence, the effective line inductance L_T is 250 μH. Since L_T reduces, I_{max} in Case II is larger than that of Case I. Theoretically, I_{max} is

$$I_{max} = I_{trip} + \frac{V_{dc}}{L_T}T = 875 + \frac{750}{250 \times 10^{-6}}100 \times 10^{-6} = 1175A. \tag{6.6}$$

The MCB is opened when the line current reaches 875 A, Fig 6.7 (a). After 100 μs, the DC line current I_{dc} reaches 1150.5 A, Fig 6.7 (e), and I_{dc} is commutated and become I_c, Fig 6.7 (c). From Fig 6.7 (b) and Fig 6.7 (d), the NoS is 6 in case II. Hence, the total energy to be dissipated W_T in Case II is less than that of Case I. The same as previous case, V_{dc}, Fig 6.7 (f), decreases during the fault interruption. The total interruption is 0.963 ms in Case II. Therefore, the performance of ACV DC-HCB in Case II also meets the requirements.

Case III, Fig 6.8, considers that the fault current is applied closed to the inverter side, which indicates the effective inductance in this case to be 10 μH. The same as pervious two cases, When I_{dc} reaches 875 A, the MCB opens and the main commutation switch T_{com} turns on. Hence the DC line current I_{dc} commutates to the commutation path and become I_c, Fig 6.8 (c). In this case, the line current I_{dc} reaches up to 6870 A, which is much larger than 1200 A, Fig 6.8 (e). From Fig 6.8 (b) and Fig 6.8 (d), the NoS is 6 which is the same as that of Case II. During the fault, V_{dc} rapidly decreases as shown in Fig 6.8 (e). After the fault interruption, V_{dc} still decreases until the PI control of the LVDC system starts to bring back the voltage to its reference value. The total interruption time is 0.283 ms. However, I_{max} of case III is much larger than 1200 A. Therefore, the performance of the ACV DC-HCB in Case III does not meet the requirement.

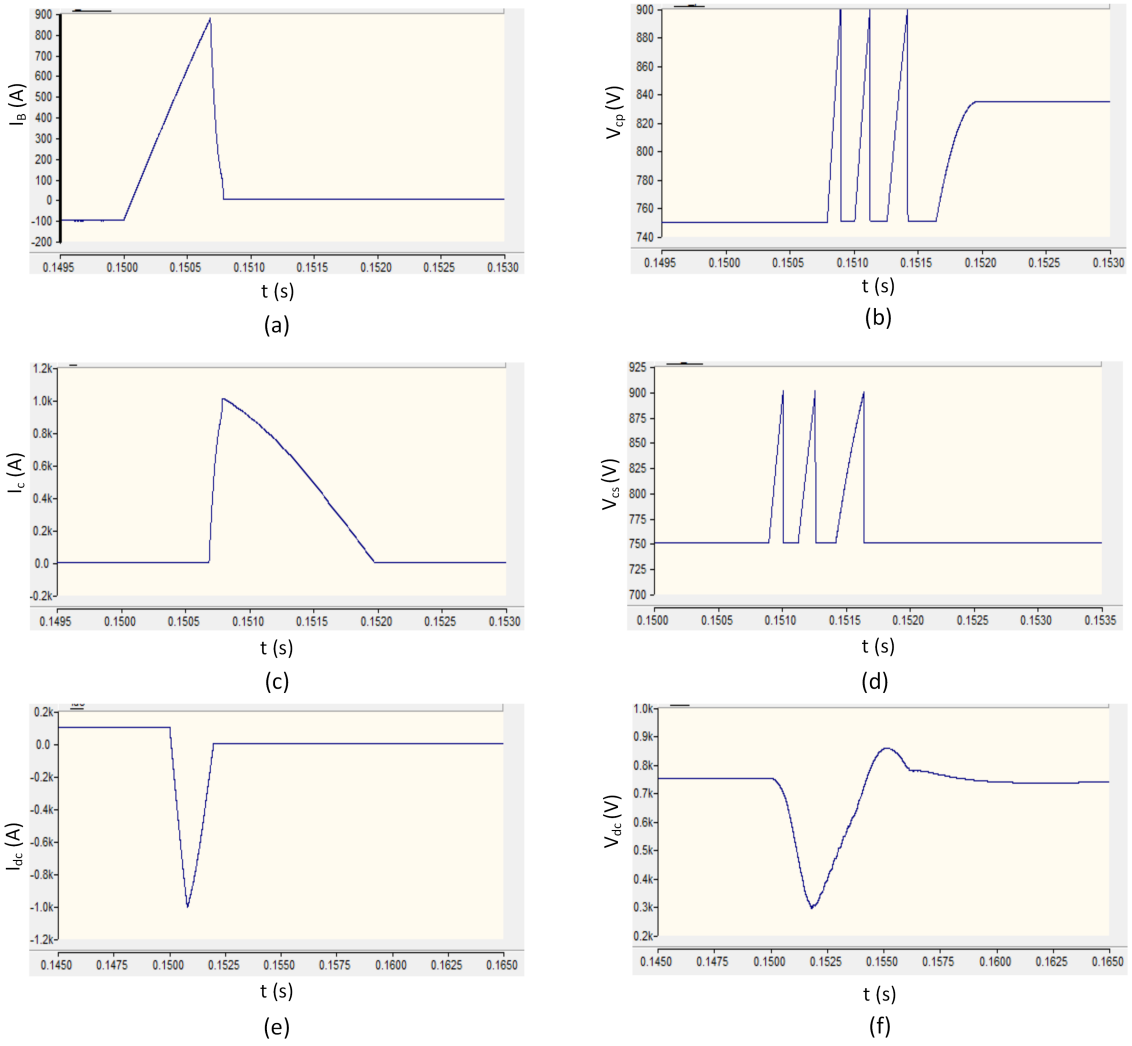

Figure 6.6: Case I: PSCAD/EMTDC simulation waveforms of the DC-HCB and the DC cable, (a) I_B vs T when DC fault applied at the rectifier side, (b) V_{cp} vs T when DC fault applied at the rectifier side, (c) I_c vs T when DC fault applied at the rectifier side, (d) V_{cs} vs T when DC fault applied at the rectifier side, (e) I_{dc} vs T when DC fault applied at the rectifier side, and (f) V_{dc} vs T when DC fault applied at the rectifier side.

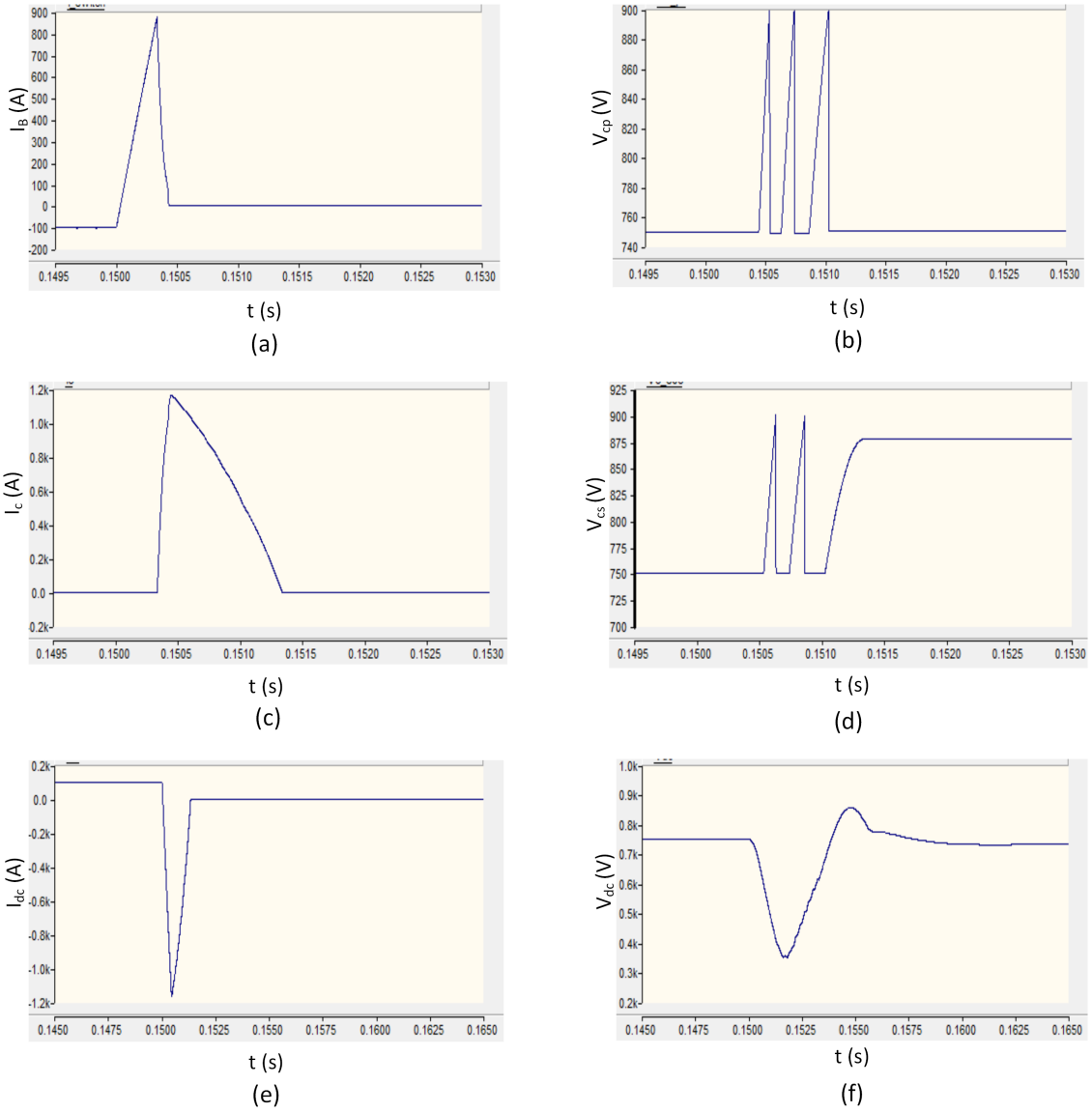

Figure 6.7: Case II: PSCAD/EMTDC simulation waveforms of the DC-HCB and the DC cable, (a) I_B vs T when DC fault applied at the middle of DC line, (b) V_{cp} vs T when DC fault applied at the middle of DC line, (c) I_c vs T when DC fault applied at the middle of DC line, (d) V_{cs} vs T when DC fault applied at the middle of DC line, (e) I_{dc} vs T when DC fault applied at the middle of DC line, and (f) V_{dc} vs T when DC fault applied at the middle of DC line.

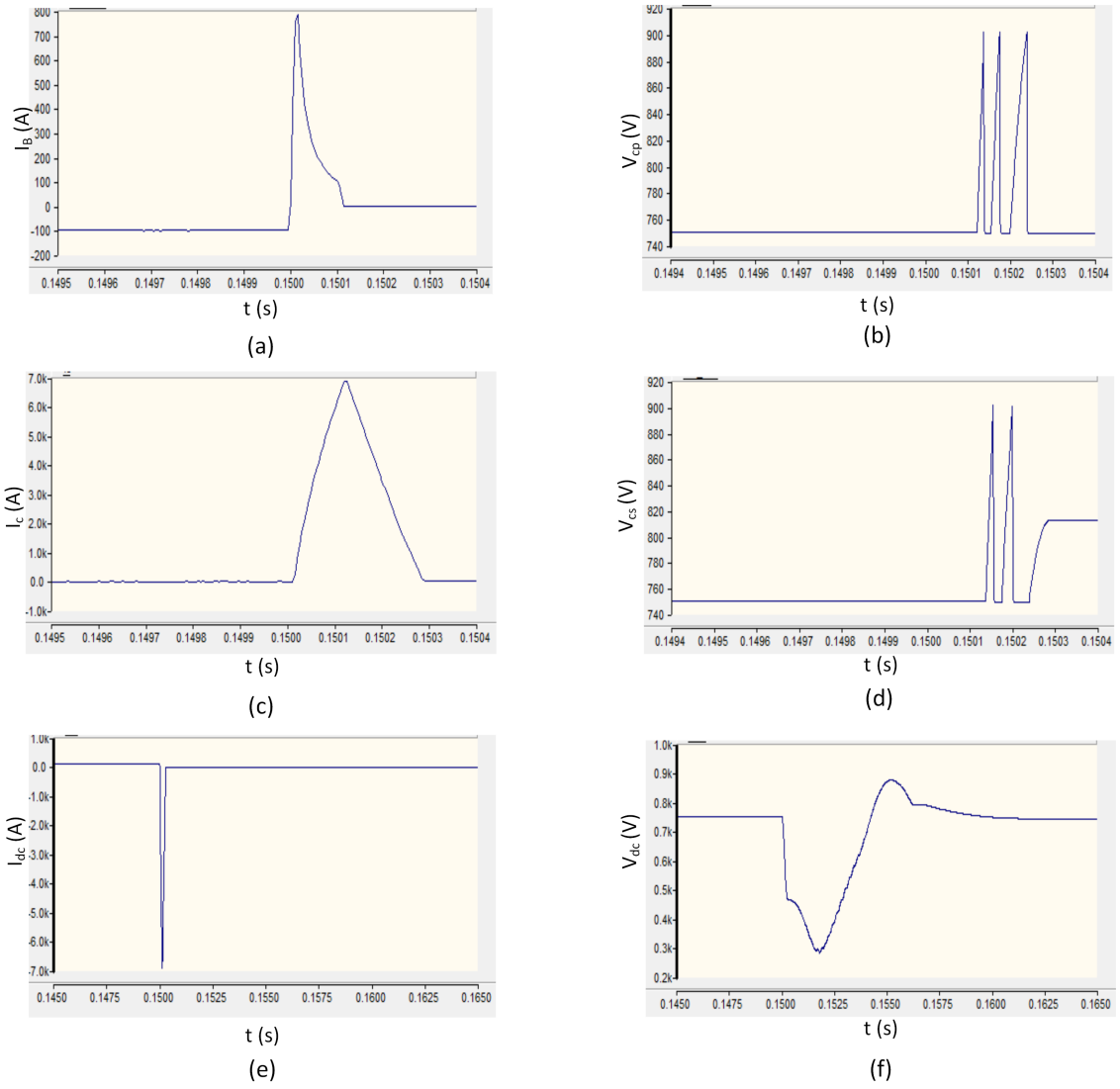

Figure 6.8: Case III: PSCAD/EMTDC simulation waveforms of the DC-HCB and the DC cable, (a) I_B vs T when DC fault applied closed to the converter, (b) V_{cp} vs T when DC fault applied closed to the converter, (c) I_c vs T when DC fault applied closed to the converter, (d) V_{cs} vs T when DC fault applied closed to the converter, (e) I_{dc} vs T when DC fault applied closed to the converter, and (f) V_{dc} vs T when DC fault applied closed to the converter.

For the ACV DC-HCB, the line current keeps increasing when the MCB starts to open until the DC arc is extinguished. From (6.5), if L_T is small, I_{max} is large regardless of the value of I_{trip}. This results in a large current went through the DC line as well the switches in the commutation path. Thus the performance of the proposed ACV DC-HCB does not meet the requirement when the effective line inductance L_T is low. If the maximum

DC line I_{max} is set at 1200 A, the lowest effective inductance (L_{Tmin}) and the minimum distance away from the proposed DC-HCB (l_{min}) can be approximated as

$$L_{Tmin} = \frac{V_{dc}}{\Delta i}T = \frac{V_{dc}}{I_{max} - I_{trip}}T = 230.77\mu H, \tag{6.7}$$

$$l_{min} = l_t - \frac{L_{Tmin}}{L_c} = 2 - \frac{230.77}{250} = 2 - 0.923 = 1.077km. \tag{6.8}$$

In (6.7), it is considered V_{dc} is constant during the fault interruption. In (6.8), l_t is the total cable length.

6.5 Conclusion

This chapter first compared the active DC-HCB with the proposed ACV DC-HCB. From the comparison, the ACV DC-HCB is a preferred option to the active mode DC-HCB. The advantages of the ACV DC-HCB compared to the active mode DC-HCB are that i) lower V_{max} and I_{max} can be achieved, ii) smaller capacitance with one single bank can be selected and iii) lower K_a can be selected. Then, Section 6.3 introduces the procedures to selected a proper ACV DC-HCB to interrupt the DC fault up to 5 kA within 5 ms as the system voltage is up to 1 kV. From Section 6.3, we demonstrate that the ACV DC-HCB is capable of performing the proper current interruption when the system inductance is large (500 μH). Finally, Section 6.4 focused on the performance evaluation of the proposed DC-HCB in the LVDC study system. From the simulation studies of Section 6.4, the performance of the ACV DC-HCB does not meet the required pattern of behavior when L_T is low (below 240.77 μH) because the maximum line current exceeds the our pre-defined limit, which may result in damaging the switches and the system devices.

Overall, the ACV DC-HCB provides the superior performance to both of the active mode DC-HCB and the traditional counter-voltage (TCV) DC-HCB. The ACV DC-HCB is capable of performing the proper current interruption when the line inductance is large, however its performance does not meet the required behavior when the line inductance is negligible.

Chapter 7

Conclusions and Future Work

The absence of natural current zero-crossing makes the interruption of DC more challenging than that of AC. The main requirements of DC interruption indicate that: i) the interruption process to be less than 5 ms, ii) the over-voltage during the CB operation to be low enough to comply with the DC system requirements and the rated value of the electronics switches, and iii) the sizes, weights and the cost of the CBs to be within acceptable limits. Based on these requirements, an alternative counter-voltage DC-HCB is proposed.

This thesis also reports extensive studies to evaluate and compare the performance of the existing/investigated DC-HCBs, i.e., the active mode DC-HCB, the traditional counter-voltage (TCV) DC-HCB, and the proposed alternative counter-voltage (ACV) DC-HCB. Principles of operations and dynamic performance of each DC-HCB are discussed. The studies are conducted based on digital time-domain simulation approach in the PSCAD/EMTDC software platform. Each DC-HCB model included the details of the corresponding component models including the DC arc model.

The feasibility studies shows that the ACV DC-HCB is the preferred DC-HCB relative to other two DC-HCBs, as well as the DC-CB without the commutation path. The merits of the ACV DC-HCB include: i) low over-voltage due to the CB operation, ii) low commutation capacitance, and iii) low dielectric strength requirement for the MCB. Based on this conclusion, we selected the parameters of a ACV DC-HCB which is capable to interrupt the DC up to 5 kA within 5 ms when the source voltage is of up to 1 kA and the system inductance is 500 μH. The identified ACV DC-HCB has applications in low-voltage DC microgrids and apparatus that are electronically coupled to the power distribution grid, e.g., utility-grade battery storage units. Performance evaluation of the ACV DC-HCB

shows that the ACV DC-HCB meet the required interruptional requirements even when the line inductance is relatively very large.

In addition to introducing and investigating a new DC-CB topology, i.e., ACV DC-HCB, another contribution of the work is that a time-domain simulation model for the DC arc also incorporated in the DC-HCB study models.

The studies conclude that the proposed ACV DC-HCB is superior to the active mode DC-HCB and the TCV DC-HCB. The ACV DC-HCB is capable of performing the proper current interruption for a wide range of line inductance values.

7.1 Future work

Potential future work in continuation of the reported studies of this thesis includes:

- Experimental performance verification of the proposed ACV DC-HCB

- Selection of the optimal component ratings and switching characteristics of the ACV DC-HCB to provide the desired performance at the minimum overall cost of the ACV DC-HCB for a given class of applications.

Bibliography

[1] R. F. Ammerman, S. Member, T. Gammon, P. K. Sen, and J. P. Nelson, "DC-Arc Models and Incident-Energy Calculations," vol. 46, no. 5, pp. 1810–1819, 2010.

[2] R. D. Garzon, *High Voltage Circuit Breaker*, 2nd ed. New York: Marcel Dekker, INC, 2002.

[3] D. Andersson and A. Henriksson, "Passive and Active DC Breakers in the Three Gorges-Changzhou HVDC Project," no. 2, 2001.

[4] A. Nabavi, "DC/AC Hybrid Circuit Breaker."

[5] K. Sano and M. Takasaki, "A Surge-Less Solid-State dc Circuit Breaker for Voltage Source Converter based HVDC Transmission Systems," *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4426–4431, Sep. 2012.

[6] C. M. Franck, "HVDC Circuit Breakers: A Review Identifying Future Research Needs," *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998–1007, Apr. 2011.

[7] A. Atmadji, "Hybrid Switching: A Review of Current Literature," *Energy Management and Power*, vol. 2, pp. 683–688, 1998.

[8] H. Nakao, Y. Nakagoshi, M. Hatano, and T. Koshizuka, "D . C . Current Interruption in HVDC SF6 Gas MRTB by Means of Self-Excited Oscillation Superimposition," *IEEE Transactions on Power Delivery*, vol. 16, no. 4, pp. 687–693, 2001.

[9] K. a. Corzine and R. W. Ashton, "A New Z-Source DC Circuit Breaker," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2796–2804, Jun. 2012.

[10] J. Mu, L. Wang, and J. Hu, "Analysis and Design of Topological Structure for DC Solid-State Circuit Breaker," *2009 World Non-Grid-Connected Wind Power and Energy Conference*, pp. 1–5, Sep. 2009.

[11] G.-c. T. Igcts, J.-m. Meyer, and A. Rufer, "A DC Hybrid Circuit Breaker With Ultra-Fast Contact Opening and Integrated," *IEEE Transactions on Power Delivery*, vol. 21, no. 2, pp. 646–651, 2006.

[12] A. Atmadji, "Direct Current Hybrid Breakers: a Design and its Realization," 2000.

[13] P. Peltoniemi, P. Nuutinen, and J. Pyrhonen, "Observer-Based Output Voltage Control for DC Power Distribution Purposes," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1914–1926, Apr. 2013.

[14] P. Schavemaker and L. V. der Sluis, "The Arc Model Blockset," *Proceedings of the Second IASTED International Conference*, pp. 644–648, 2002.

[15] S. Nitu, C. Nitu, and C. Mihalache, "Comparison between Model and Experiment in Studying the Electric Arc," *JOURNAL OF OPTOELECTRONICS AND ADVANCED MATERIALS*, vol. 10, no. 5, pp. 1192–1196, 2008.

[16] X. Xun, "Investigate on the Simulation of Black-box Arc Model," *Electric Power Equipment - Switching Technology (ICEPE-ST),*, no. 1, pp. 629–636, 2011.

[17] J. Paukert, "The Arc Voltage and Arc Resistance of LV Fault Arcs," *Proc. 7th Int. Symp. Switching Arc Phenom.*, pp. 49–51, 1993.

[18] H. Ayrton, "The Electric Arc," *U.K.: Electrician*, 1902.

[19] W. B. Nottingham, "A New Equation for the Static Characteristic of the Normal Electric Arc," vol. 203, no. 1904, pp. 302–310, 1923.

[20] A. D. S. W. T. Oppenlander, "Electric arcs in Open Air," vol. 26, 1991.