Control and Operation of a Utility Grid Connected DC Fast Charging $$\operatorname{Station}$$

by

Zhi Jin Zhang

A thesis submitted in conformity with the requirements for the degree of Master of Applied Science Graduate Department of Electrical and Computer Engineering University of Toronto

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Abstract

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Zhi Jin Zhang Master of Applied Science Graduate Department of Electrical and Computer Engineering University of Toronto 2019

This thesis investigates the impact and the performance of a grid-connected DC fast charging station (DCFCS) in a rural distribution system. The fast charging station consists of three DC fast chargers (DCFCs), each of which is rated at 800 V and 360 kW. The studies are conducted in time-domain using the off-line PLECS software. It is observed that, in the uncontrolled charging scenario, the lowest short-circuit ratios (SCRs) the charging station can operate in, without violating the system voltage drop constraint, are 7.1 under 2% unbalanced grid and 6.4 under balanced grid conditions. Subsequently, a curtailment scheme and a supervisory control strategy utilizing a battery energy storage system (BESS) are proposed to extend the DCFCS' operational SCR limit down to 4.0 in a 2% unbalanced grid. Both off-line and real-time simulation results verify that the BESS-enhanced DCFCS is able to operate under the extended grid SCR condition.

To my parents

Acknowledgements

I would like to express my gratitude to all the individuals who provided me with help and encouragement. Without them, my thesis journey could be much harder.

Specifically, I am deeply indebted to Professor Reza Iravani, who gave me the opportunity to conduct research in his group starting from my undergraduate thesis. His wisdom and expertise have been valuable to me throughout these years and I am honored to have worked under his supervision.

I am grateful to Dr. Milan Graovac and Mr. Xiaolin Wang for their insightful instructions and feedback on my research, which are very beneficial.

I would like to thank Professor Zeb Tate and Professor Ali Hooshyar for reviewing my thesis and providing useful suggestions, and Professor W. Murray Wonham for chairing my oral examination.

My lab colleagues, Arman Ghasaei, Mostafa Mahfouz, and Mubarek Abdela, have made the last two years fun and memorable. I will not forget our stimulating discussions, eventful soccer matches, and countless strolls around the campus.

Last but not least, I want to give my special thanks to my parents; without their support, this thesis could not be completed.

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Acronyms

BESS Battery Energy Storage System. BMS Battery Management System. **CC** Constant Current. CCM Continous Conduction Mode. ${\bf CV}\,$ Constant Voltage. DCFC DC Fast Charger. **DCFCS** DC Fast Charging Station. ${\bf EMI}$ Electromagnetic Interference. **EV** Electric Vehicle. FC Fast Charger. **HF** High Frequency. **IGBT** Insulated-Gate Bipolar Transistor. LC Local Controller. LF Line Frequency. LPF Low-Pass Filter. LUT Look-Up Table. **MOSFET** Metal-Oxide-Semiconductor Field-Effect Transistor. NERC North American Electric Reliability Corporation. NF Notch Filter. PCC Point of Common Coupling.

- **PI** Proportional-Integral.
- $\ensuremath{\textbf{PLL}}$ Phase-Locked Loop.
- ${\bf PWM}\,$ Pulse-Width Modulation.
- ${\bf RMS}\,$ Root Mean Square.
- **SC** Supervisory Controller.
- SCHIL Supervisory Control Hardware-in-the-Loop.
- ${\bf SCR}$ Short-Circuit Ratio.
- ${\bf SHB}$ Sample-and-Hold Block.
- **SOC** State of Charge.
- **TDD** Total Demand Distortion.
- **THD** Total Harmonic Distortion.
- \mathbf{VCO} Voltage-Controlled Oscillator.
- ${\bf VSC}$ Voltage-Sourced Converter.

Chapter 1

Introduction

This chapter provides the background and motivation for the study of operation of a utility grid connected DC fast charging station, followed by a literature review of the subject area. Next, the thesis objectives are introduced and an overview of the rest of the thesis is provided.

1.1 Background and Motivation

Interests in electric vehicles (EVs) have grown owing to environmental concerns; thanks to the concerted effort from both academia and automotive industry, EVs are becoming a viable alternative to gasoline-powered automobiles for commuters. Battery charger is identified as one of the required technologies for EVs, and providing a proper charging methodology can greatly facilitate electric vehicle usage and alleviate the so-called "range anxiety". An EV charger can be classified according to its location (on- or off-board), the power it provides (level 1, 2, or 3), and its electrical output (AC or DC) [2]. An overview of the classification is depicted in Fig. 1.1.



Figure 1.1: Classification of EV chargers.

An EV with an on-board charger directly connects to an AC outlet and the charging process, including AC to DC conversion, is done inside the vehicle. A minimal amount of off-board service equipment is required since the power electronics for charging are located on-board. In comparison, off-board chargers alleviate the necessity of AC to DC conversion on-board and they directly provide the requested DC charging current to EV batteries. As the name suggests, all power electronic components are located

outside of the EV and the off-board location relaxes the converters' volume and weight requirement. As a result, the charging power of an off-board charger is typically much higher than that of an on-board charger.

EV charging power can be categorized into three levels. Level 1 charging power is rated below 1.92 kW, level 2 up to 19.2 kW, and level 3 is designated for power above 20 kW [2]. Level 1 charging is generally achieved by plugging into any wall outlet supplied by a single-phase AC line. Since the output voltage and current from a wall outlet are AC quantities, level 1 charging is also classified as AC charging. In comparison, a level 2 charger can have its power delivered by single, double, or three-phase lines and consists of a dedicated electrical box and cord as its off-board service equipment to ensure safety. Nonetheless, the level 2 charging cord still outputs AC quantities and it is still AC charging. Lastly, level 3 charging is almost exclusively associated with off-board charging compared to the other two levels owing to the amount of power it can deliver. Level 3 charging is typically supplied by threephase AC lines, but AC to DC conversion is accomplished in an off-board fashion; thus, its output electrical quantities are DC. Also, since level 3 charging power is greater than levels 1 and 2, it greatly reduces the charging time. Hence, level 3 charging is often referred to as DC fast charging and a level 3 off-board charger is called a DC fast charger (DCFC). Note that level 3 AC on-board fast charging also exists; however, owing to the power electronics required on-board to process the large amount of power, it is still an active research area and infrequently appears in the EV charging vernacular compared to DC fast charging.

There are four DC fast charging standards used by EV manufacturers: SAE Combo Charging System (CCS), CHAdeMO, Tesla Supercharger, and GB/T, with the latter two being exclusively applied to Tesla stations and charging stations in China, respectively [3]. Previously, CHAdeMO and and CCS standards have specified their upper fast charging limits to be 62.5 kW and 80 kW, respectively. Nonetheless, the limits have been raised to 400 kW (CHAdeMO 2.0) and 350 kW (CCS 2.0) in 2018 [4, 5], due to the advancements in EV battery and power converter technologies. With each DCFC able to dispense up to 400 kW and charging station power rating potentially increasing to MW level in the foreseeable future, it is imperative to ask:

- 1. What is the impact of MW level fast charging on an AC utility grid, especially in rural distribution systems along highway stops these DCFCs are most likely to be installed?
- 2. What is limiting a fast charging station's grid operating range, i.e., lowest short-circuit ratio (SCR)?
- 3. How can engineers reduce fast charging footprint on a utility grid and extend the operating limit of the fast charging station?

Note that a charging station's grid impact has a negative effect on its grid operating range, which means that by reducing the grid impact, the operating range can be increased.

1.2 Literature Review

As grid penetration of electric vehicles grows, the charging demand may pose significant challenges to grid capacity and operation. The power system component that is most likely to be adversely affected by EV load has been identified in the technical literature as the distribution network and the three major impacts are (1) peak power demand [2, 6], (2) voltage sag [7, 8], and (3) harmonic distortion [9, 10].

Two different charging philosophies have been proposed in the technical literature [2]. The first approach is called controlled charging. In this scenario, an EV can only charge at certain times of a day and/or with a pre-determined charging power. These restrictions may be generated through optimization algorithms in order to minimize the total generation cost and network losses, reduce peak demand, etc [11, 12, 13]. Nevertheless, the state-of-the-art optimal charging models do not consider voltage deviation while charging and require a significant amount of computation time [13, 14]. Another example of controlled charging is rule-based power admission control that accepts or rejects EV charging requests based on charging priority and grid constraints, i.e., on-off control [15, 16]. However, the particular discrete-event approach adopted by authors in [15, 16] overlooks the possibility of providing partial power and may increase the overall charging time.

In comparison, EVs are charged with their requested amount of power whenever they want in uncontrolled charging scenarios. This approach is more compatible with DC fast charging since fast charging is more time-critical and unpredictable compared to slow charging in residential environments. However, additional energy storage and/or reactive power devices are necessary to prevent feeder overload and voltage drop while satisfying the power demand [2, 17]. Overall, with respect to DC fast charging, controlled approach can be favored by grid operators while EV customers may prefer uncontrolled approach. Many solutions demonstrated in the technical literature use a combination of these two philosophies.

Battery energy storage systems (BESS) appear to be a viable choice for mitigating DC fast charging station (DCFCS) impact because BESS can reduce EV load demand seen from the grid by acting as an energy buffer; as a result, they (1) contribute to grid voltage regulation, (2) prevent system overload, (3) allow the charging station owner to avoid peak demand charges, and (4) deliver ancillary services [18, 19]. A strategy utilizing both charging schedule optimization and BESS integration was proposed in [20], where the objectives were cost reduction and peak power suppression for electric bus charging. Nevertheless, since the buses ran with fixed routes and times, it was relatively easy to profile load behavior and generate the optimal charging schedule, which may not be achieved for vehicles charging along highways. In [21], each DCFC was integrated with two battery storage systems to partially decouple the DCFCS from a utility grid and BESS charging/discharging was determined based on their state of charge (SOC) values and EV load; however, the authors did not consider changes in the grid condition while charging and their DCFCs were only rated at 70 kW.

Reference [9] investigated voltage and current total harmonic distortion (THD) and total demand distortion (TDD) caused by commercially available DCFCs and has concluded that harmonic limitation was the primary binding condition of DCFC operations, but the type of power converter being tested was not mentioned. Authors in [10] proposed an active filter to attenuate AC side harmonics for a DCFC with a diode rectifier front end. However, harmonic issues can be reduced if an active front end, instead of a diode rectifier, is used [22].

Bidirectional power flow capabilities [17, 23] and renewable energy integration [24, 25] are also demonstrated to be capable of mitigating grid impact and providing ancillary services; nonetheless, they are not included in the scope of this thesis and can be considered in future works.

Although a considerable number of case studies exist on identifying and mitigating the grid impact of fast charging stations, very few authors have focused on charging stations of MW level and none has fully conducted a comprehensive performance evaluation to examine both voltage and harmonic distortions, let alone augmenting a charging station's grid operating range. This research attempts to develop, assess, and enhance an 1 MW DC fast charging station in a utility grid in order to address this gap.

1.3 Thesis Objectives

The purpose of this thesis is to investigate and mitigate the impact of an 1 MW DC fast charging station on a distribution level utility grid in order to extend the charging station's grid operating range. The fast charging station is comprised of three DC fast chargers, each of which is rated at 360 kW. The number of DCFCs in the charging station is three so that (1) the charging station power rating is approximately 1 MW and (2) group effect, rather than two-body coupling effect, can be examined. As mentioned above, bidirectional power flow capabilities and renewable energy integration are not in the scope of this work. Furthermore, long-term and system-wide generation and load profiling is not studied. The specific objectives are:

- 1. Develop a realistic model for a 360 kW DCFC to enable the study of DC fast charging in an AC grid.
- 2. Evaluate the performance and the impact of the charging station under different grid conditions and identify its grid SCR limit.
- 3. Extend the charging station's operating limit by mitigating its grid impact.

Note that upgrading the power system infrastructure is an obvious, albeit costly and unrealistic, solution to the above-mentioned problem and this option will not be considered.

1.3.1 Methodology

The following steps are taken to fulfill the objectives of this thesis:

- 1. Select a DCFCS architecture and the associated AC host system.
- 2. Design and select appropriate DCFC circuit parameters and power electronic converter topologies.
- 3. Define the charging voltage and current range of the DCFC and implement a local controller (LC) that is able to work in this range and ride through unintentional faults.
- 4. Investigate, in the PLECS off-line simulation software, the performance of the charging station consisting of three DCFCs under balanced and unbalanced grid voltages with a viable range of SCR values.
- 5. Evaluate the fault ride-through behavior of the charging station under line-to-line-to-ground (LLLG) and single-phase line-to-ground (LG) faults.
- 6. Based on the outcome of the previous two steps, identify the lowest SCR for the grid-connected charging station to be functional in uncontrolled charging scenarios and the source of this limitation, i.e., voltage or harmonic distortions.
- 7. Devise a strategy for extending the existing SCR operating limit of the fast charging station without integrating a BESS, i.e. a controlled charging strategy.

- 8. Extend the SCR limit by integrating a BESS and devise a supervisory control (SC) strategy to coordinate BESS and DCFCS operations
- 9. Verify if the proposed strategies fulfill their objectives in the off-line simulation, and then implement the BESS-enhanced DCFCS system in a RTDS-based hardware-in-the-loop testbed to demonstrate hardware implementation feasibility.

Note that detailed power electronics design and optimization, e.g., efficiency and thermal studies, are not in the scope of this thesis; only a functional and feasible design in the electrical domain is provided.

1.3.2 Study System Description

This section introduces possible architectures for a DC fast charging station, namely, how individual chargers interface with the AC utility grid, and describes the rural distribution AC grid that hosts the fast charging station. This effectively completes Step 1 of Section 1.3.1

DC Fast Charging Station Architecture

For safety reasons, each charger is required to provide isolation of the battery pack from the rest of the charging network [2, 26, 27]. Hence, depending on the location of the galvanic isolation, which is provided by a transformer, two types of off-board charging structures are possible. In the first type, the isolation transformer is situated between the utility grid and the charger, and all chargers connect to a common AC bus as shown in Fig. 1.2(a); because the transformer directly operates at the grid frequency, this structure is called the line-frequency (LF) isolation architecture. The second type addresses the isolation requirement by placing the transformer at the DC-DC stage, where the DC-DC converter first performs DC to AC conversion, albeit to a frequency much higher than the grid frequency, and then rectifies the electrical quantities back to DC again. Since the transformer operates at a high frequency, this structure is named the high-frequency (HF) isolation architecture. The HF architecture can be implemented in two different ways as depicted by Figs. 1.2(b) and 1.2(c). In the common AC bus concept, the architecture is similar to its LF counterpart except the transformer is located in the DC-DC conversion stage. In the common DC bus concept, there is only one centralized AC-DC conversion unit, and multiple isolated DC-DC converters share the same DC bus. To the best of the author's knowledge, there is no indication of superiority of a particular charging architecture in terms of grid-connected performance.

The DC fast charging station investigated in this thesis adopts the LF architecture, which only needs non-isolated DC-DC stages compared to the HF architecture [2, 28]; non-isolated converters are known to be more efficient and less costly than their isolated counterparts.

The major drawback for the LF architecture is that these transformers tend to be bulky [28]. However, because the fast charging stations are regarded as the equivalent to gas stations, they are unlikely to be installed in residential areas, and will be seen in places such as major highway stops. Hence, land usage is not likely to be a significant concern for fast chargers. In addition, LF transformers can be bought off-the-shelf, whereas HF transformers often need to be customized. Depending on economic viability, commonality may be a better design choice than customization. The LF isolation architecture also offers redundancy because if one of the chargers is malfunctioning, the others will still be operational.



(a)



(b)



Figure 1.2: General off-board charging station architectures: (a) LF isolation, (b) HF isolation with a common AC bus, and (c) HF isolation with a common DC bus.

AC Host System

The AC system is a realistic rural distribution feeder with a voltage rating of 27.6 kV (line-to-line, RMS), which is the standard voltage level for Toronto Hydro distribution feeders. The feeder is 26 km long and its overhead line, load, and transformer parameters are displayed in Tables A.2 to A.4, respectively. The designed DC fast charging station is connected to the bus B16 on the feeder as indicated in Fig. 1.3.



Figure 1.3: Single-line diagram of the rural distribution feeder.

1.4 Thesis Layout

The remainder of this thesis is organized into five chapters:

Chapter 2 presents the selection of DCFC transformer, power electronic converter topologies, converter parameters, and design of the charger's LC. Particularly, for the AC-DC converter, fault ride-through strategy is discussed, and for the DC-DC converter, eigenvalue sensitivity analysis is performed for the local controller with respect to EV battery parameter variations. This chapter corresponds to Steps 2 and 3 of Section 1.3.1.

Chapter 3 provides the in-depth performance evaluation of the DC fast charging station in PLECS. EV battery model for simulation is explained and two charging points of interest are identified. The lowest SCR values for the charging station to remain operational under balanced and unbalanced grid voltage conditions are found via progressively lowering the short-circuit ratio until the charging station violates system constraints. Fault ride-through behavior is also studied. This chapter fulfills Steps 4 to 6 of Section 1.3.1.

Chapter 4 proposes a curtailment scheme for extending the SCR limit of the charging station and devises a supervisory control strategy for BESS integration to share real and reactive powers between the charging station and the BESS. It demonstrates the viability of the proposed strategies through a set of nine comprehensive off-line simulation case studies. This chapter accomplishes Steps 7 and 8 and off-line simulation part of Step 9 of Section 1.3.1.

Chapter 5 demonstrates the hardware implementation of the supervisory control in a hardware-inthe-loop real-time simulation structure. The purpose of this study is to consider physical effects such as communication delay and digitization error in the simulation and investigate the functionality of the charging system as it is subjected to various continuous- and discrete-time events. Disagreements between the real-time and off-line simulation results are discussed. This chapter completes real-time simulation part of Step 9 of Section 1.3.1.

Chapter 6 concludes the thesis by summarizing the work done in previous chapters, highlighting the contributions, and presenting possible future works for extending such a study.

Chapter 2

DC Fast Charger Modeling and Control

This chapter describes modeling and local control of a DCFC. Sections 2.1 to 2.3 present transformer selection, and design and control of the AC-DC and DC-DC stages of a DC fast charger.

2.1 Transformer Selection

As mentioned in Section 1.3.2, each charger is connected to the 27.6 kV rural feeder through an isolation transformer. This transformer steps down the voltage from 27.6 kV to 0.6 kV (line-to-line, RMS), which is the input voltage to the following AC-DC stage. It has a grounded wye configuration on the high voltage side and delta configuration on the low voltage side. Since each charger is rated at 360 kW, the transformer power rating is selected to be 0.45 MVA. The typical percent impedance (Z%) for transformers of this rating is 4.12, and the X/R ratio is 3.85 [29]. The no-load loss percentage is chosen to be 0.086% [30]. This type of transformer is available off-the-shelf. The transformer parameters are summarized in Table 2.1.

Table 2.1. Isolation transformer ratings.									
Roting (MVA)	Phoeoe	I	Iigh Voltage	I	Low Voltage	Impedance (%)	X/R Ratio	Core Power Loss (%)	
maning (WWA)	1 mases	kV	Configuration	kV	Configuration				
0.45	3	27.6	Grounded Wye	0.6	Delta	4.12	3.85	0.086	

Table 2.1: Isolation transformer ratings

2.2 AC-DC Conversion Stage

The AC-DC stage consists of an input filter and an AC-DC converter (rectifier). Selection of the converter topology and filter parameters, and local control of the converter are discussed in this section.

2.2.1 Converter Topology

The AC-DC converter is responsible for AC to DC conversion and is often required to operate at unity power factor [2]. Vienna rectifier is a popular topology which contains a low number of active switches (one per phase) and is easy to control practically (e.g. no two active switches per leg removes dead-time problems) [2, 31]. Nevertheless, a more prevalent technology in industry is the three-phase, two-level voltage-sourced converter (VSC). The VSC is composed of six switching cells, typically realized by IGBTs, a DC capacitance, and three line inductors. The VSC switching circuit is depicted in Fig. 2.1, whereas Fig. 2.2 shows the placements of the DC side capacitor (C_{DC}) and AC side line inductors (L_f). The turn on/off commands are typically issued by pulse-width modulation (PWM) signals. A main feature of employing the VSC is that it is a more economically viable option compared to other choices owing to its industry ubiquity.



Figure 2.1: A three-phase VSC switching circuit.

2.2.2 Parameter Selection

Since each charger is rated at 360 kW, the power rating for the VSC is selected to be 0.4 MVA. For proper sinusoidal PWM operation, the switching frequency of the converter is chosen based on [32]:

$$f_{carrier} = 3n f_{system} \qquad n = odd. \tag{2.1}$$

The parameters f_{system} and n, in (2.1), are 60 Hz and 35, respectively, making the switching frequency to be 6300 Hz.



Figure 2.2: VSC connection to an AC system.

The LC filter, as indicated in Fig. 2.2, is used to reduce harmonic components generated by switching

actions. The inductance value is selected to be 15% of its base value: $L_f = 15\% \times L_{base} = 358.1 \ \mu H$. The capacitance value is chosen to be 20% of its base value: $C_f = 20\% \times C_{base} = 589.5 \ \mu F$. These two base quantities are determined based on converter nominal values, and are presented in Table A.1. Hence, the corner frequency of the LC filter is:

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}} = 346.40 \ Hz$$

The aforementioned switching frequency is 6300 Hz; this makes the filter cutoff frequency to be approximately 18 times lower than the switching frequency, which is desirable for attenuating switching harmonics.

The internal power loss associated with the inductor can be represented by an equivalent resistance. This loss is defined by the quality factor (Q) of the inductor:

$$Q = \frac{\omega L}{R} = \frac{X_L}{R}.$$
(2.2)

For the inductor in this filter, it is assumed to have a high quality factor (Q = 75), and as a result, the internal resistance of the inductor is $r_f = 1.8 \ m\Omega$. The DC-link capacitor value is chosen to be $C_{DC} = 5000 \ \mu F$ [33, 24].

2.2.3 Local Controller Design

The local controller for the VSC should satisfy two objectives based on the power exchange between the AC and DC sides of the VSC: (1) DC voltage regulation and (2) unity power factor operation. Either voltage or current can be used for power control; however, current control is preferred since controlling the voltage can expose the VSC to overcurrent. Therefore, it is a common practice to track reference current set-points [34].

The VSC current and voltage controllers are implemented in the synchronous (dq0) reference frame, where the angle ρ for the transformation from $\alpha\beta$ -frame to dq-frame is obtained by a phase-locked loop (PLL). The PLL is a control system by itself which forces the quadrature component of the AC side voltage, v_{sq} , to be 0 in the steady-state [34]. The advantages of transformation to dq-frame are that the real and reactive powers can be decoupled and the control variables are DC values under quasisteady-state conditions. Furthermore, if the PLL is in steady-state, then the real and reactive powers are directly proportional to i_{td} and i_{tq} , which are the direct and quadrature components of the VSC terminal current (i_t in Fig. 2.2), respectively [34]. This means that to achieve the aforementioned two objectives, one only needs to control i_{td} for regulating the DC voltage and i_{tq} for achieving unity power factor operation. Hence, it is imperative to have a well-designed PLL.

Phase-Locked Loop Design

A control block diagram of the PLL is shown in Fig. 2.3 [34, 35]. Since the loop gain already has an integral term, in the form of a voltage-controlled oscillator (VCO), only one more integrator is needed to track ramp signals with zero steady-state error. However, under unbalanced grid voltage and fault conditions, a significant double line frequency (120 Hz) AC component will exist in v_s due to the presence of negative-sequence voltage components. Hence, a 120 Hz notch filter (NF), NF(s), is included [35], in



Figure 2.3: Control block diagram of the PLL with the low voltage bypass mechanism.

order to synchronize to the positive-sequence voltage. The NF has a form [36] of

$$NF(s) = \frac{s^2 + \omega^2}{s^2 + \frac{\omega s}{Q} + \omega^2},\tag{2.3}$$

where Q and ω are chosen to be 10 and 754 rad/s, respectively.

The compensator L(s) is generated based on the procedure provided in [34]:

$$L(s) = \frac{2.68 \times 10^5 (s^2 + 568516)(s^2 + 166s + 6889)}{s(s^2 + 1508s + 568516)(s^2 + 964s + 232324)} \ [rad/s],$$

and the output of L(s) is limited between $2\pi(55)$ and $2\pi(65)$. Note that L(s) has a unit of [rad/s] instead of [(rad/s)/V] owing to the per-unit system used for VSC control.

Lastly, a low voltage bypass structure [35] is also implemented for fault situations where v_s drops so low that the PLL would have trouble of tracking its phase. The bypass structure calculates the magnitude of v_s , given by $|v_s| = \sqrt{v_{sd}^2 + v_{sq}^2}$, whose value is passed to a hysteresis block such that when $|v_s| < 0.2 \ p.u$, the effect of the PLL controller is nullified and a constant signal of $2\pi(60)$ is fed into the VCO to produce ρ ; as soon as $|v_s|$ becomes greater than 0.4 p.u, the bypass mechanism reactivates the PLL compensator and switches the VCO input signal back to the output of L(s).

Current Controller Design

The block diagram of the controller and the plant is shown in Fig. 2.4(a) [34]. The following assumptions are made for controller design:

- 1. DC side voltage is relatively constant over a switching period (this is satisfied by having a large enough DC-link capacitor).
- 2. There is no path for zero-sequence current to flow (this is imposed by utilizing the wye-delta transformer).
- 3. Ideal switch model is considered (this is justifiable since switching loss is small on system-level and does not affect system performance, which is the focus of this thesis).

Fig. 2.4(a) demonstrates that both the coupling of i_{td} and i_{tq} and the grid voltage disturbance input to the plant (v_{sdq}) are resolved by feedback of i_{tdq} and feedforward of v_{sdq} , respectively. Therefore, the



(a)



(b)



Figure 2.4: Block diagrams for: (a) Overall VSC current control, (b) Net view of current control, and (c) DC voltage regulation.

resultant system for i_{td} controller is depicted by Fig. 2.4(b), which is also adopted for controlling i_{tq} . The LPF

$$H(s) = \frac{1}{2.53 \times 10^{-4} \times s + 1},\tag{2.4}$$

is included in the feedback path to produce an adequately clean control signal, with a time constant chosen to be 10 times lower than the switching frequency. To attenuate the 120 Hz signal in the controller, instead of utilizing a LPF with a bandwidth lower than 120 Hz, which is known for causing instability issues [36], the notch filter in (2.3) is used in the feedback path as well. However, the feedforward cross-coupling cancellation signals i_{tdq} and v_{sdq} are not equipped with a notch filter since the AC grid frequency is assumed to be constant [36, 37].

The compensator $k_d(s)$ is a PI controller to track DC variables with zero steady-state error. Using MATLAB SISO Design Tool, the closed-loop step response is designed to have a settling time of 11.6 ms and an overshoot of 0.8%. The addition of the 120 Hz NF in the controller makes the response more oscillatory. The final $k_d(s)$ is

$$k_d = \frac{0.1s + 0.8}{s} \ [\Omega]$$

Since the control loop is the same, $k_q(s)$ is identical to $k_d(s)$.

Unity Power Factor Operation



Figure 2.5: Unity power factor operation mechanism.

To maintain the power factor at unity at the low voltage side of the isolation transformer, i_{tqref} is set to be the quadrature component of the capacitor current i_C as indicated by Fig. 2.5. A second-order LPF expressed by

$$W(s) = \frac{2.5 \times 10^7}{s^2 + 8000s + 2.5 \times 10^7}$$

and the 120 Hz NF of (2.3) are used to filter out switching and double line frequency harmonics for i_{Cq} .

Furthermore, a P-priority current limiter is implemented for i_{tqref} to ensure the VSC terminal current does not exceed its rated value, i_{rated} , which is set to 1.1 *p.u.* The P-priority limiter calculates $\sqrt{i_{td}^2 + (i_{Cq}^{filtered})^2}$ and compares the result to i_{rated} . If $\sqrt{i_{td}^2 + (i_{Cq}^{filtered})^2} > i_{rated}$, then i_{tqref} is set to $\sqrt{i_{rated}^2 - i_{td}^2}$, else $i_{tqref} = i_{Cq}^{filtered}$. The priority is given to real power during normal operations, and the limiter will be disabled during fault conditions.

DC Voltage Regulation

The DC-side voltage is regulated at 1 kV and a fairly constant DC voltage is maintained as the input to the DC-DC conversion stage. There are two methods for controlling the DC-link voltage:

- 1. Design a compensator to generate i_{td} reference value from the DC voltage error signal. Since all quantities are DC, this compensator can be a PI controller [38]. This structure's block diagram is depicted in Fig. 2.4(c).
- 2. Design a controller that uses the DC voltage error signal to adjust the real power set-point accordingly so that the DC capacitor net power exchange is zero [34].

Owing to the adequacy and simplicity of the first method, it is implemented to control the DC-link voltage. In Fig. 2.4(c), T(s) is the closed-loop expression for i_{td} current controller, v_{sd}^n is the nominal peak line-to-neutral voltage value which is equal to $\frac{600 \times \sqrt{2}}{\sqrt{3}} \approx 489.90 V$, and V_{DC}^n is the nominal DC voltage of 1000 V. Similar to the current controller, a NF of (2.3) is added in the feedback to attenuate the 120 Hz component in the control signal.

However, due to the inclusion of the NF, design of the compensator involves making trade-offs between damping and stability margins of the controller. The PI compensator $k_v(s)$ is chosen to be slower than the inner current loop controller, i.e.,

$$k_v = \frac{3.5s + 35}{s} \ [\Omega^{-1}].$$

The outer voltage closed-loop system has a gain margin of 9.1 dB and a phase margin of 36.4 degrees.

Moreover, a fault bypass block is implemented for the DC voltage regulator as depicted in Fig. 2.4(c). Once the grid fault is detected, the voltage compensator is deactivated and the reference signal for the inner current loop, i_{tdref} , is set to 0 by the bypass structure. The voltage controller is reactivated when the fault is cleared. The reason for regulating i_{td} to 0 will be explained next.

Fault Ride-Through Capability

When the AC system is subjected to a disturbance, e.g., a fault, its protection system would adhere to fault ride-through characteristics with respect to frequency and voltage. In this thesis, the AC grid is assumed to be strong enough to allow frequency disturbance to be overlooked. The voltage ride-through time duration curve from the North American Electric Reliability Corporation (NERC) requirement [39] is adopted in this thesis, as depicted in Fig. A.1.

Since voltage drop occurs during faults, low voltage ride-through (LVRT) logic should be implemented as a part of the VSC local controller so that the VSC can (1) remain energized during faults with normal clearing (4 to 9 cycles) [39] (LVRT-1), (2) provide a reactive current amounting to at least 2% of the rated current for each percent of the voltage drop within 20 ms after fault detection [40] (LVRT-2), (3) limit current overshoot of IGBTs to a maximum of 20% of the rated current (LVRT-3), and (4) limit the overshoot of DC-bus voltage to a maximum of 20% of the blocking voltage of the DC-DC converter's power semiconductor switching devices (LVRT-4). Both fault detection and LVRT mechanisms are implemented in each DCFC to demonstrate the charging station's fault ride-through capability.

The fault detection mechanism is depicted in Fig. 2.6. Normally, the AC bus protective relay is able to report a fault occurrence; however, the communication delay between the relay and the VSC can

range from 2 to 8 ms, which is significant compared to the fault duration. Therefore, a secondary layer of detection is done within the VSC local control, which calculates $|v_{PCC}|$, point of common coupling (PCC) voltage, and inputs the value into a hysteresis block, such that when the voltage magnitude is below 0.65 *p.u.*, the block outputs a value of 1, and once the voltage rises above 0.9 *p.u.*, the hysteresis block outputs 0. The overall fault detector decision is based on the two mechanisms: (1) protective relay signal (the actual relay is not simulated in this thesis, but is assumed to exist in the study system with a communication latency) and (2) low voltage detection (LVD) structure; the detector logic is implemented in a state machine in the VSC local controller such that it outputs fault_detected = 1 (fault happened) as soon as any of these two mechanisms raises a fault flag, then after a delay of two cycles, which is used to prevent multiple transitions, the state machine checks whether the fault is cleared, which is represented by an output of fault_detected = 0. This ensures the fault detection occurs as fast as possible so that the local controller can react early during a fault.



Figure 2.6: Fault detection mechanism.

After a fault is detected, the original inputs to i_{tdref} and i_{tqref} , coming from DC-link voltage and unity power factor regulators, are disabled, and the DC-DC converter is deactivated. i_{tdref} will be instead assigned as 0 because when voltage drops significantly, it is not desirable to further exacerbate the problem by drawing more active power from the utility grid. Simultaneously, LVRT AC bus voltage controller, presented in Fig. 2.7, is activated; it compares the reference $|v_{PCC}|$ set-point, which is equal to 1 *p.u.*, with the measured value, and the error is passed through a proportional controller to generate i_{tqref} . The proportional controller, P(s), is used to emulate the droop behavior between AC voltage and reactive power; it has an expression of

$$P(s) = -2 \ [\Omega^{-1}],$$

to fulfill the requirement that 2% of the rated VSC current shall be injected for every percent drop of the AC bus voltage. Since i_{tdref} is set to 0, there is no need to implement a Q-priority current limiter because the VSC current is now solely reserved for i_{tq} . A 120 Hz NF of (2.3) and a first-order LPF of (2.4) are used to attenuate second-order and switching harmonics in $|v_{PCC}|$.

Note that $\alpha\beta$ -frame voltages are used to calculate $|v_{PCC}|$, instead of dq-frame values, to avoid transient errors arising from the transformation angle ρ . In addition, when the voltage $|v_{PCC}|$ is between 0.65 and 0.9 *p.u.* as a result of a fault upstream in the AC system, the protective relay is assumed to be able to identify the fault occurrence, since this condition does not trigger the low voltage detection mechanism owing to its hysteresis structure.



Figure 2.7: LVRT AC bus voltage controller.

PWM Strategy

A sinusoidal PWM strategy [34, 32] is adopted for the VSC. The local controller outputs signals v_{tdq} , which are divided by $\frac{V_{DC}}{2}$, and then transformed back to *abc*-frame to obtain three switching signals m_{abc} ; they are compared with a carrier triangular waveform of 6300 Hz to generate gating signals for the switches of the VSC.

2.3 DC-DC Conversion Stage

Due to a diverse range of electric vehicles, a DCFC needs to supply power at different operating voltage conditions. For instance, Porsche Taycan, which goes into production in 2019, is able to charge at 350 kW at a voltage level up to 800 V [41, 42], and Tesla Model S charges at 400 V with a maximum of 100 kW charging power [43].

It is known that for a sinusoidal PWM driven VSC operating in the linear region (amplitude modulation ratio $m_a \leq 1.0$), the line-to-line RMS voltage ($V_{LL, RMS}$) is related to the DC-link voltage (V_{DC}) by [32]:

$$V_{LL, RMS} = \frac{\sqrt{3}}{2\sqrt{2}} m_a V_{DC} \approx 0.612 m_a V_{DC}.$$
 (2.5)

For the DCFC designed in this thesis, the AC side of the VSC is connected to the secondary side of the isolation transformer. Therefore, $V_{LL, RMS}$ is equal to 600 V, and based on (2.5), the DC-side voltage of the VSC has a minimum value of 980 V. The VSC DC output cannot be directly used as a charger port; this necessitates a dedicated DC-DC converter as the charger output to enable the fast charger to be compatible with a variety of electric vehicle batteries.

The next three sections provide the design procedure for the DC-DC converter including topology and output filter selections, the formulation of local controllers, and lastly, sensitivity analysis with respect to the plant uncertainties.

2.3.1 Converter Topology

A number of DC-DC converters suitable for DC fast charger implementation have been discussed in the technical literature. Conventional non-isolated topologies such as buck, boost, buck-boost, and Cuk have been compared in [28] and [44]. A solution based on cascaded H-bridge multilevel converter is proposed in [45], where each sub-module is a full-bridge DC-DC converter and can be connected to an electric vehicle. The advantages of using a multilevel converter include low component stress and reduced filter size. However, the control circuit can be complex. A series resonant matrix converter topology is presented in [46], where a matrix converter provides a high-frequency sinusoidal output that is fed into a resonant tank and eventually converted to DC quantities. This alleviates the need for the VSC since the matrix converter can directly interface with the utility grid; however, because no monolithic bidirectional switches exists, this topology requires additional switching components that increases overall cost and complexity.

For this thesis, it is justifiable to assume that the output charging voltage is always less than 1 kV (the converter input voltage regulated by the VSC), given the fact that the aforementioned Porsche Taycan, the only EV to the best of the author's knowledge that can charge around the rated power this fast charger is designed for, charges up to 800 V. Therefore, the buck converter is a viable topology. This is a simple and reliable topology to work with and has a high efficiency [2, 28, 44]. Moreover, due to the relatively high level of power (current) the converter needs to deliver, interleaving technique should be considered [47, 48], where the current demand is shared by the interleaved phases/legs. Also, if a phase-shift control algorithm is applied, meaning adjacent phases are driven by gate drive signals phase shifted by $\frac{360^{\circ}}{N}$ where N is the number of legs, the output current and voltage will have an effective frequency of the switching frequency multiplied by N and their ripples will be greatly attenuated, which decreases the passive component sizes [2, 49]. Thus, interleaving resolves the trade-off issue between switching loss and efficiency. Other benefits of interleaved buck topology is selected for this application.

The next topology design decision is selection of the number of phases for the buck converter. Authors in [48] present an interleaved buck converter for a fast charger rated at 220 kW that is composed of 11 phases in order to achieve a current ripple below 2% relative to the nominal output current. In [47], it is stated that the state-of-the-art engineering for the electric vehicle charger application uses three to five paralleled buck phases to build the converter. The same paper also implements 16- and 36-leg buck converters. However, this thesis proposes to use a three-phase synchronous interleaved buck converter, which has a switching circuit as depicted by Fig. 2.8. This topology is termed synchronous buck due to the substitution of the free-wheeling diode that exists in the basic buck converter circuit by another active switching device such as IGBT or MOSFET [51]. Each leg of the converter constitutes a basic buck converter switching circuit. The reason for choosing this particular topology is that it has the same layout as a voltage-sourced converter (cf. Fig. 2.1). Thus, similar to a VSC, this converter structure is available off-the-shelf.



Figure 2.8: A 3-phase interleaved buck converter switching circuit.

2.3.2 Parameter Selection

Output voltage and current ripples at EV side are limited to a maximum of 5% to prevent degradation of EV batteries [27]. The design specifications of the DC-DC converter are shown in Table 2.2. Note that the per phase current ripple limit of 30% is not as stringent as the total current ripple (5%) because of the ripple cancellation in the interleaved configuration. Hence, the size of the inductors per phase can be reduced. In addition, the converter output current is assumed to be high enough during steady-state that only continuous conduction mode (CCM) needs to be considered in all subsequent design decisions.

Parameter	Minimum Value Typical Value Maximum Value							
Input voltage	1000							
Output voltage	300	800	800	V				
Output voltage ripple (peak-to-peak)		$5\% \times 300 = 15$		V				
Output current	90	435	450	A				
Output current ripple (peak-to-peak)		$5\% \times 90 = 4.5$		A				
Output current per phase	30	145	150	A				
Output current ripple per phase (p-p)		$30\% \times 30 = 9$		A				

Table 2.2: Buck converter steady-state design specifications.

The switching frequency is chosen at 20 kHz. This design choice preferably requires silicon-carbide (SiC) MOSFETs instead of IGBTs since the switching losses of IGBTs are significantly higher at such a switching frequency [52, 53]. The minimum ratings of the SiC switches, based on Table 2.2, should be 1.2 kV and 400 A [54]. Based on the selected switching frequency, the output inductor and capacitor are determined.

Fig. 2.9 presents the output side of the buck converter with its connection to an EV battery. The reverse current prevention diode, required by [26], stops reverse current flowing to the on-board battery. The battery model is composed of a controlled voltage source (V_b) behind a series resistance (R_b) based on [1]. If equal current sharing can be achieved for all legs of the buck converter, the per phase inductors will have the same inductance value [49]. For one phase of the buck converter, the peak-to-peak inductor current ripple, $\Delta i_{Lj, pp}$, where j = 1, 2, 3, is given by [55]:

$$\Delta i_{Lj, pp} = \frac{v_C(1-D)}{f_s L_j},$$
(2.6)



Figure 2.9: Buck converter connection to an EV battery.

where v_C is the output capacitor voltage, D is the duty cycle, f_s is the switching frequency, and L_j is the per phase inductance. (2.6) is valid under the following assumptions:

- 1. Steady-state operation: net change of energy in the inductor is 0.
- 2. Small-ripple approximation: V_{input} (generated by the VSC) and v_C are approximated by their respective DC components with ripples neglected.
- 3. V_{input} is relatively constant.
- 4. Converter loss is ignored.

The duty cycle for a buck converter is the ratio of the output voltage to the input voltage, and since the input voltage is assumed to be fixed at 1 kV, D can be expressed as: $D = \frac{v_C}{1000}$. Therefore, the numerator of (2.6) can be translated to $v_C \times (1 - \frac{v_C}{1000})$.

For each phase, it is allowed a worst-case peak-to-peak current ripple of 9 A. And it can be observed that the worst-case scenario occurs at $v_C = 500 V$ when the numerator of (2.6) is maximized. Substitute $v_C = 500 V$ in (2.6), the inductance value is determined as

$$L_j = \frac{500 \times (1 - \frac{500}{1000})}{20 \times 10^3 \times 9} = 1.3889 \ mH \approx 1.4 \ mH,$$

where j = 1, 2, 3.

With the inductance value determined, it is necessary to verify whether or not the peak-to-peak ripple of the total inductor current (i_t in Fig. 2.9) obtained by superposition of all three phase shifted inductor currents is within the allowable limit. This steady-state ripple can be expressed by [49, 51]

$$\Delta i_{t, pp} = \frac{v_C (1 - \frac{m}{ND})(1 + m - ND)}{f_s L_j} = K_{NORM} \times K_{RCM}, \qquad (2.7)$$

where m = floor(ND) (the floor function), $K_{NORM} = \frac{v_C}{f_s L_j}$, and $K_{RCM} = v_C(1 - \frac{m}{ND})(1 + m - ND)$ (called the ripple current cancellation multiplier). Note that K_{RCM} is always less than 1 for duty cycles between 0 and 1, which suggests that the total inductor current ripple is less than the ripple from each

phase. A MATLAB script was written to plot the total inductor current ripple against the output voltage, which is presented in Fig. 2.10.



Figure 2.10: Variation of the total inductor current ripple.

Fig. 2.10 shows that the output current ripple does not vary linearly with the output voltage owing to the interleaving structure, and the worst-case scenario ripple occurs when $v_C = 500 V$ and has a value of $\Delta i_{t, pp} = 2.98 A$. This is smaller than the permissible ripple of 4.5 A in Table 2.2. Note that this is a conservative calculation since the limit of 4.5 A is actually imposed on the output charging current i_{out} in Fig. 2.9, which is even less than i_t . Hence, the charging current ripple is within the prescribed limit.

The output capacitor voltage ripple is expressed by [55]

$$\Delta v_{C, pp} = \frac{\Delta i_{t, pp}}{4N f_s C}.$$
(2.8)

This is valid under the following assumptions:

- 1. Steady-state operation: net change of energy in the capacitor is 0.
- 2. Small-ripple approximation: V_{input} is DC. It is also relatively constant.
- 3. Converter loss is ignored.

The maximum permissible ripple is 15 V, while the current maximum permissible ripple is 4.5 A (2.98 A is not used to have a more conservative estimation). Hence, the output capacitance value is $C = 1.25 \ \mu F$. However, the smallest off-the-shelf DC-link capacitor rated for 1 kV that can be found is 2 μ F [56]; this commercially available value is chosen for the output capacitor.

2.3.3 Local Controller Design

The DC-DC converter interfaces with the EV battery to provide current and voltage defined by the EV's battery management system (BMS). The three conventional methods that the converter can deliver power to the battery are: constant current (CC), constant voltage (CV), and constant current-constant voltage (CC-CV) [2]. The first/second method requires the charger to supply a current/voltage level specified by the BMS throughout the charging process, but neither provides overvoltage/overcurrent protection for the battery. The CC-CV method solves this issue by employing CC charging during the initial charging phase to protect against overcurrent when a large amount of charging current is required; then when the

battery's state of charge (SOC) reaches a predefined level, typically 80%, it switches to CV charging to offer overvoltage protection and allow the charging current to decrease exponentially. A current profile during CC-CV charging is shown in Fig. 2.11.



Figure 2.11: Sample current profile during CC-CV charging.

In another fast charging technique, the battery is charged with current pulses that can be negative (discharging) and/or with variable frequency, which are aimed to increase charge acceptance and provide a more accurate SOC estimation [57]. Nevertheless, whether pulse charging is actually beneficial for electric vehicle batteries is still an active research area; therefore, it is not adopted in this thesis.

The CC-CV technique is implemented, which means the DC-DC local controller needs to satisfy the following objectives:

- 1. Provide a constant output current as requested by the battery BMS.
- 2. Provide a constant output voltage as requested by the battery BMS.
- 3. Transition seamlessly between constant current mode and constant voltage mode as requested by the battery BMS.
- 4. It is insensitive to load (battery) variables.

These objectives are satisfied by assuming the converter input voltage is relatively constant and utilizing a cascaded control structure where the inner/outer loop is for current/voltage control, respectively. This structure is explained in detail in the following sections.

Current Controller Design

Referring to Fig. 2.9, the charging current (i_{out}) to be controlled is the sum of inductor currents (i_t) , assuming the average capacitor current (i_C) is zero over one switching period. Hence, this thesis proposes to regulate i_{out} by controlling the output currents of each phase of the buck converter independently, which achieves both charging current regulation and current sharing. The control structure is illustrated in Fig. 2.12; it depicts that the BMS reference current (i_t^{ref}) is divided by the number of converter legs to obtain set-points for each phase, and then passed to the current controllers to generate gate drive signals for each half-bridge leg. Note that the phase-shift control strategy is implemented in the PWM circuits residing in the current controllers, where the 20 kHz sawtooth waveforms of legs 2 and 3 are phase shifted by 120° and 240° , respectively, compared to leg 1.


Figure 2.12: Current control structure.

Controlling each phase independently also alleviates the need to derive the overall small-signal model for the interleaved converter; instead, the per phase small-signal model can be calculated using the AC modeling approach [55] to design the current controller (e.g. PI) for all three control loops in Fig. 2.12. The small-signal model for one leg of the interleaved buck converter including the equivalent battery model is presented in Fig. 2.13(a), where v_g , d, i_L , and v_b are the perturbations on input voltage V_{input} (or V_g), duty cycle D, inductor current I_L , and battery internal electromotive force V_b , respectively; L is the per phase inductor, C is the output capacitor, and R_b is the battery internal resistance. For convenience, it is denoted that $d = d_1 = d_2 = d_3$ (phase shift in duty cycles does not affect controller synthesis), $L = L_1 = L_2 = L_3$, and $i_L = i_{L1} = i_{L2} = i_{L3}$, so Fig. 2.13(a) is applicable for all three legs of the converter. Also, it should be noted that since each phase only supplies $\frac{1}{3}$ of the total current, the equivalent output impedance (C and R_b) should be scaled as seen from each phase. Hence, the small-signal model shows $\frac{C}{3}$ and $3R_b$ [51].

Assuming the system has reached the quiescent operating point the small-signal model is valid for, the control (d) to output (i_L) transfer function $G_{id}(s)$ can be derived by setting both v_g and v_b to zero (valid under the assumptions that the input voltage is constant and battery voltage variation is slow) as shown in Fig. 2.13(b).

Thus, based on Kirchhoff's Voltage Law:

$$i_L(s) = \frac{V_g d}{sL + \frac{3}{sC} || (3R_b)} = \frac{V_g d}{sL + \frac{3R_b}{1+sCR_b}},$$
(2.9)

and from (2.9)

$$G_{id}(s) = \frac{i_L}{d} = \frac{V_g(sCR_b + 1)}{s^2 LCR_b + sL + 3R_b} \ [A].$$
(2.10)

The PWM transfer function is $G_{PWM}(s) = \frac{1}{V_M} [V^{-1}]$ where V_M is the peak-to-peak amplitude of the sawtooth waveform, which is equal to 1 in this work. Based on the transfer functions, the current control block diagram for one leg of the converter is depicted in Fig. 2.14(a) (note that a LPF is included in the current feedback path to reduce switching harmonics in the control signal). One important feature to



Figure 2.13: Small-signal models for: (a) Single-phase buck, and (b) Transfer function derivation.

observe is that if the closed-loop expression for a single leg current controller from i_L^{ref} to i_L is denoted as T(s), then the overall control structure in Fig. 2.14(b) can be reduced to that of Fig. 2.14(c)

$$i_t(s) = \frac{i_t^{ref}}{3}T(s) + \frac{i_t^{ref}}{3}T(s) + \frac{i_t^{ref}}{3}T(s),$$

and

$$\frac{i_t}{i_t^{ref}} = \frac{i_L}{i_L^{ref}} = T(s).$$
(2.11)

This indicates that the closed-loop expression for the interleaved buck converter current controller is identical to the transfer function of a single phase controller. (2.11) will be used to obtain the outer loop voltage controller.

The LPF is chosen as a first-order filter

$$G_{fb}(s) = \frac{1}{\tau_i s + 1},$$
(2.12)

where the time constant τ_i is 10 times lower than the switching frequency of $40000\pi \ rad/s$, i.e., $\tau_i = 7.96 \times 10^{-5} \ s$.

The compensator is a PI controller and using MATLAB SISO Design Tool, the closed-loop step



Figure 2.14: Block diagrams for: (a) Single-phase current control, (b) Three-phase current control, and (c) Simplified overall current control structure.

response is designed to have a settling time of 2.4 ms and an overshoot of 2.4%. It has the form of

$$c_i(s) = \frac{\frac{2}{450}s + 1}{s} \ [\Omega]. \tag{2.13}$$

The controller is designed based on $V_g = 1000$ and L and C values given in Section 2.3.2, and R_b is 60 $m\Omega$. However, R_b is an uncertain plant parameter that varies in the order of tens of $m\Omega$ depending on the battery type and operating conditions; therefore, a sensitivity analysis is conducted, using the converter small-signal model, to evaluate its impact.

Eigenvalue Sensitivity Analysis for Current Controller

The EV battery internal resistance, R_b , can vary depending on temperature, SOC, and battery chemistry. Since the current controller is designed around the nominal resistance of 60 $m\Omega$, an eigenvalue sensitivity analysis is performed to investigate the effects of plant parameter uncertainty on system stability. In this analysis, trajectories of the closed-loop system eigenvalues are plotted as R_b changes.

In the single phase small-signal model displayed in Fig. 2.13(b), two differential equations based on the inductor current and capacitor voltage can be written as:

$$L\frac{di_L}{dt} = V_g d - v_C, \qquad (2.14)$$

$$\frac{C}{3}\frac{dv_C}{dt} = i_L - \frac{v_C}{3R_b}.$$
(2.15)

Note that (2.14) and (2.15) also can be expressed as

$$\frac{di_L}{dt} = \frac{V_g}{L}d - \frac{v_C}{L},\tag{2.16}$$

$$\frac{dv_C}{dt} = \frac{3}{C}i_L - \frac{v_C}{CR_b}.$$
(2.17)

The state-space form is constructed, where the internal state variable, $x \in \mathbb{R}^{2 \times 1}$, is equal to $\begin{bmatrix} i_L \\ v_C \end{bmatrix}$:

$$\dot{x} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{3}{C} & -\frac{1}{CR_b} \end{bmatrix} x + \begin{bmatrix} \frac{V_g}{L} \\ 0 \end{bmatrix} u,$$

$$y = \begin{bmatrix} 1 & 0 \end{bmatrix} x,$$
(2.18)

where $u = \frac{d}{G_{PWM}(s)} = d$ as depicted in Fig. 2.14(a).

The feedback filter of (2.12) can be expressed in state-space form as:

$$\dot{\theta} = -\frac{1}{\tau_i}\theta + i_L,$$

$$i_{Lf} = \frac{1}{\tau_i}\theta,$$
(2.19)

where θ is an internal state variable and i_{Lf} is the filtered inductor current. For brevity, the expression $-\frac{1}{\tau_i}$ is designated as a in all future references.

Let i_{Ld} be the reference inductor output current to be tracked $(i_L^{ref}$ in Fig. 2.14(a)); from the current controller block diagram, it is apparent that u is the output of the PI controller, which is

$$u = k_I \times \left(\int_0^t [i_{Ld}(\tau) - i_{Lf}(\tau)] d\tau\right) + k_P \times (i_{Ld} - i_{Lf}),$$
(2.20)

where k_I and k_P are integral and proportional coefficients in (2.13), respectively. Denote $\xi = \int_0^t [i_{Ld}(\tau) - i_{Lf}(\tau)] d\tau$, then clearly $\dot{\xi} = i_{Ld} - i_{Lf} = i_{Ld} + a\theta$ and $u = k_I \xi + k_P \dot{\xi} = k_I \xi + k_P a\theta + k_P i_{Ld}$.

Hence, the internal state variable, x, can be augmented to incorporate the new variables θ and ξ , becoming a vector:

$$z = \begin{bmatrix} x \\ \theta \\ \xi \end{bmatrix} = \begin{bmatrix} i_L \\ v_C \\ \theta \\ \xi \end{bmatrix},$$

and the new state-space expression becomes:

$$\dot{z} = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{ak_P V_g}{L} & \frac{k_I V_g}{L} \\ \frac{3}{C} & -\frac{1}{CR_b} & 0 & 0 \\ 1 & 0 & a & 0 \\ 0 & 0 & a & 0 \end{bmatrix} z + \begin{bmatrix} \frac{k_P V_g}{L} \\ 0 \\ 0 \\ 1 \end{bmatrix} i_{Ld},$$

$$y = \begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix} z,$$
(2.21)

where y is the variable of interest, which is equal to i_L , and the input to the system is the current set-point i_{Ld} .



Figure 2.15: Trajectories of eigenvalues for the current controller as battery internal resistance varies.

Trajectories of the four eigenvalues of the transition matrix (or the so-called A matrix) in (2.21) are plotted in Fig. 2.15 for R_b varying between 1 $m\Omega$ and 500 $m\Omega$, which is the most extreme worst-case range estimate. The first eigenvalue in Fig. 2.15(a) decreases to approximately a minimum of -10^6 as R_b increases, and its magnitude is always the largest among the four eigenvalues; hence, its effect is minimal on controller performance. Both eigenvalues in Figs. 2.15(b) and 2.15(c) vary between -5000and -7000, and the eigenvalue analysis shows that they introduce oscillatory behavior to the system as R_b increases. The speed of the controller is dominated by the fourth eigenvalue in Fig. 2.15(d), which is the smallest among the four. Overall, all eigenvalues have negative real parts for the range of the battery internal resistance investigated, which indicate that the system is stable when subjected to these variations.

Note that the sensitivity analysis plots the eigenvalues of A instead of the the poles of the corresponding closed-loop transfer function T(s) since:

$$\{eigenvalues of A\} \supset \{poles of T(s)\}.$$

Thus, the stability of the system is guaranteed if all eigenvalues of A are in the left half of the complex plane, and the converse is not necessarily true.

Voltage Controller Design

It is necessary to control the output voltage v_C during CV charging stage; this thesis proposes to add an outer voltage control loop in addition to the current control as shown by Fig. 2.17(a), where the controller $c_v(s)$ generates current set-points constantly from the voltage error signal, similar to VSC DC voltage regulation loop.



Figure 2.16: Converter output port small-signal model.

To obtain the expression for $G_{vi}(s)$, one simply needs to look at the output part of Fig. 2.13(b) as depicted in Fig. 2.16. Note that as seen by i_t , the output impedances are in their original values and do not need to be multiplied by 3

$$G_{vi}(s) = \frac{v_C}{i_t} = \frac{R_b}{sCR_b + 1} \ [\Omega].$$
 (2.22)

Based on the same nominal parameters used for determining the current controller, the voltage controller is

$$c_v(s) = \frac{s+1000}{s} \ [\Omega^{-1}]. \tag{2.23}$$

It is slower than the inner loop controller with a step response settling time of 67.9 ms and an overshoot of 0%.

Now the transition mechanism between the voltage and current modes is investigated. Due to the cascaded structure, switching from voltage to current mode is simple, where only a current set-point step change is involved, meaning the set-point is changed from the output of the voltage controller to an external reference. This transition does not necessitate any modification to the existing structure and also has the fast response the current controller is designed to provide. However, the transition











(c)

Figure 2.17: Block diagrams for: (a) Voltage control, (b) Voltage control with transition mechanism, and (c) CC-CV overall control structure.

from current to voltage mode is problematic because of (1) the anti-windup mechanism in the voltage controller and (2) the speed of the voltage controller is slower than its current counterpart. To explain, imagine when the DC-DC converter is tracking a non-zero constant current i_t^{ref} when a request is made to change to voltage control mode. Due to the anti-windup mechanism, the voltage controller has a zero output immediately before the mode transition; then this PI controller is activated and produces a non-zero signal. Nonetheless, since the current controller is much faster than the voltage controller, it first tracks the zero output reference generated by the voltage compensator at the moment the transition is made and continuously follows the ensuing non-zero set-points from the voltage controller. Hence, a large undershoot is produced as the result during current to voltage transition.

The solution proposed by this thesis to mitigate the transition undershoot is illustrated by Fig. 2.17(b). Comparing this block diagram to the one in Fig. 2.17(a), the difference is that a feedforward term of i_t^{ref} is added to the output of the voltage compensator. When the mode transition command is sent, this signal activates a sample-and-hold block (SHB) such that the block locks the last value of i_t^{ref} before the switch and the new current reference $(i_t^{ref'})$ is composed of this constant DC value along with the output of $c_v(s)$. This mechanism ensures the inner loop reference does not deviate greatly before and after the transition, which resolves the aforementioned problem. In the actual CC-CV charging process, the purpose of the voltage control is to hold the output voltage immediately before the mode transition constant, so it is not necessary to move to another voltage set-point; this is achieved by employing an additional SHB which is also initiated by the mode switching signal as demonstrated by Fig. 2.17(c). Note that the feedforward mechanism is even more beneficial for the actual CC-CV control structure by relieving the stress on the voltage controller. Moreover, because this feedforward term is a constant input DC bias, it does not affect the performance of the PI controller and need not to be considered in the controller design process as a result, which is another advantage of this technique.

Eigenvalue Sensitivity Analysis for Voltage Controller

The same sensitivity analysis conducted for current controller is also performed for the voltage controller by plotting the eigenvalue trajectories for the closed-loop system when subjected to variations in R_b . To obtain the state-space expression for the voltage controller, first note that the input to the system in (2.21), i_{Ld} , is generated by the PI controller of the outer voltage loop. Hence, the same technique of augmenting the state-space matrices employed for current controller analysis can be applied. Let v_d be the voltage loop set-point (v_G^{ref} in Fig. 2.17), it is apparent that

$$i_{Ld} = k_{vI} \times \left(\int_0^t [v_d(\tau) - v_C(\tau)] d\tau\right) + k_{vP} \times (v_d - v_C),$$
(2.24)

where k_{vI} and k_{vP} in (2.24) are integral and proportional coefficients in (2.23), respectively. Denote $\eta = \int_0^t [v_d(\tau) - v_C(\tau)] d\tau$, then it can be observed that $\dot{\eta} = v_d - v_C$ and $i_{Ld} = k_{vI}\eta + k_{vP}\dot{\eta}$.

The state variable, z, from (2.21) is extended to

$$z = \begin{bmatrix} i_L \\ v_C \\ \theta \\ \xi \\ \eta \end{bmatrix}.$$

The original state-space system of (2.21) now becomes:

$$\dot{z} = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{ak_{F}V_{g}}{L} & 0 & 0 & 0\\ \frac{3}{C} & -\frac{1}{CR_{b}} & 0 & 0 & 0\\ 1 & 0 & a & 0 & 0\\ 0 & 0 & a & 0 & 0\\ 0 & -1 & 0 & 0 & 0 \end{bmatrix} z + \begin{bmatrix} \frac{k_{F}V_{g}}{L} \\ 0\\ 1\\ 0 \end{bmatrix} (k_{vI}\eta + k_{vP}\dot{\eta}) + \begin{bmatrix} 0\\ 0\\ 0\\ 0\\ 1\\ 0 \end{bmatrix} v_{d} = \\ = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{ak_{F}V_{g}}{L} & \frac{k_{I}V_{g}}{L} & 0\\ \frac{3}{C} & -\frac{1}{CR_{b}} & 0 & 0\\ 1 & 0 & a & 0 & 0\\ 0 & 0 & a & 0 & 0\\ 0 & -1 & 0 & 0 & 0 \end{bmatrix} z + \begin{bmatrix} \frac{k_{F}V_{g}}{L} \\ 0\\ 0\\ 1\\ 0 \end{bmatrix} (\begin{bmatrix} 0 & 0 & 0 & 0 & k_{vI} \end{bmatrix} z + k_{vP}v_{d} - \begin{bmatrix} 0 & k_{vP} & 0 & 0 & 0\\ k_{vP} & 0 & 0 & 0 \end{bmatrix} z) + \\ & + \begin{bmatrix} 0\\ 0\\ 0\\ 0\\ 1\\ 0 \end{bmatrix} v_{d}, \\ y = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \end{bmatrix} z,$$
(2.25)

which reduces to:

$$\dot{z} = \begin{bmatrix} 0 & \left(-\frac{1}{L} - \frac{k_P k_v P V_g}{L}\right) & \frac{a k_P V_g}{L} & \frac{k_I V_g}{L} & \frac{k_P k_v I V_g}{L} \\ \frac{3}{C} & -\frac{1}{CR_b} & 0 & 0 & 0 \\ 1 & 0 & a & 0 & 0 \\ 0 & -k_v P & a & 0 & k_{vI} \\ 0 & -1 & 0 & 0 & 0 \end{bmatrix} z + \begin{bmatrix} \frac{k_P k_v P V_g}{L} \\ 0 \\ k_v P \\ 1 \end{bmatrix} v_d,$$
(2.26)
$$y = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \end{bmatrix} z,$$

where y is the capacitor voltage and the input to the system is the voltage set-point v_d . It can be seen that a duality exists between the current and voltage expressions of (2.21) and (2.26), respectively.

The trajectories of the five eigenvalues of the transition matrix of (2.26) are plotted in Fig. 2.18 when R_b varies between the worst-case range of 1 $m\Omega$ and 500 $m\Omega$. The first eigenvalue in Fig. 2.18(a) drops to approximately -10^6 as R_b increases, and the magnitude is so large that its effects are minimal on controller performance. Eigenvalues in Figs. 2.18(b) and 2.18(c) start to have imaginary components as R_b increases, which will lead to oscillatory behavior. Lastly, the fifth eigenvalue (Fig. 2.18(e)) is the smallest among all five eigenvalues of the voltage loop and four eigenvalues of the current loop, which confirms that the voltage controller is slower than its current counterpart. Moreover, it has a minimum value (approximately -3) at $R_b = 1 m\Omega$, which illustrates that a new controller may need to be designed if the charger usually operates around this resistance value. Nevertheless, an internal resistance of 1 $m\Omega$ is an extremely pessimistic estimate and is uncommon for car batteries, whose resistance values should be around tens of $m\Omega$. Thus, this analysis demonstrates that the voltage controller is insensitive to the load variable for the range defined in this section; the objectives stated in Section 2.3.3 are achieved.



Figure 2.18: Trajectories of eigenvalues for the voltage controller as battery internal resistance varies.

2.4 Conclusions

This chapter provides (1) parameter selection for a DCFC and (2) topology selection and local controller design for the AC-DC and DC-DC stages of the charger. The power electronic topologies and parameters chosen are shown to be economically viable for the charger that is rated at 360 kW. Local control strategies are developed for the AC-DC and DC-DC converters based on theories from power electronics and control systems. Fault ride-through controller is implemented in the AC-DC converter to ensure the charger can remain energized in faults with normal clearing. Eigenvalue sensitivity analysis is conducted for the local controller of the DC-DC converter in order to evaluate the impact of the EV batteries' uncertainties on converter operation. The eigenvalue trajectories show that the converter will remain stable given a wide range of EV battery internal resistances.

Chapter 3

Performance Evaluation of DC Fast Charging Station

Theoretical design of a DCFC has been conducted in Chapter 2. To evaluate and verify the performance of the DCFC's local controller and investigate the charging station's operating limits in the uncontrolled charging scenario, the DCFCS is implemented in the PLECS time-domain simulation software package and simulated under various grid conditions. This chapter is dedicated to demonstrating steady-state and transient charging behavior at two operating points of interest on the battery charging characteristic curve.

3.1 Battery Model for Simulation



Figure 3.1: Non-linear battery model reprinted from [1].

The EV battery model consists of a controlled internal voltage source (V_b) , representing the internal electromotive force, behind an internal resistance (R_b) . Designated as E in Fig. 3.1, V_b is calculated based on the SOC of the battery; its equation is depicted the same figure, where parameters E_0 , K, A, B are determined from curve fitting, and Q is the battery capacity in Ah.

The two particularly interesting operating points for the DCFC are (1) maximum power output point at 800 V and 450 A (hereafter denoted as MPOP) and (2) maximum charging current percentage ripple point at 500 V and 90 A (hereafter denoted as MROP). The reason for choosing 500 V and 90 A as MROP is because of the fact that it is more imperative to examine current ripple rather than voltage ripple since the DC-DC converter output voltage is dictated by the battery. As demonstrated by Fig. 2.10, the output current ripple is largest around an output voltage of 500 V. Also, because the ripple is only a function of output voltage, not output current, the lowest steady-state current the charger provides, namely, 90 A, is chosen to obtain the maximum current percentage ripple.

Charging at MPOP and MROP will reveal the operating limit of the charging station in uncontrolled charging scenarios. Two artificial battery models are generated, based on [58, 59, 60], so that these two operating points are already reached once the off-line simulation starts. The model for MPOP is represented by

$$V_b = E_0 - K \times \frac{Q}{Q - it} + A \times e^{(-B \times it)} = 230.3 \times (3.31 - 0.0218 \times \frac{40}{40 - it} + 0.04 \times e^{-0.0868 \times it}), \quad (3.1)$$

with a battery resistance value of $64.125 \text{ m}\Omega$.

The model for MROP is given by

$$V_b = 148.5 \times (3.31 - 0.0218 \times \frac{40}{40 - it} + 0.04 \times e^{-0.0868 \times it}), \tag{3.2}$$

with a battery resistance value of $32.063 \text{ m}\Omega$.

3.2 Performance under Non-Ideal Grid Conditions

The functionality of the station under an ideal AC grid (infinite AC bus) has been thoroughly verified; the results are shown in Appendix B.1 owing to space limitations. In this section, the performance of the grid-connected DC fast charging station under non-ideal steady-state grid conditions is evaluated. The fast charging performance under the AC grid's transient conditions, i.e., system faults, will be examined in Section 3.3. All three chargers were simulated and they received identical charging commands; the voltage and current waveforms at strategic points of each DCFC are found to be the same. Hence, only one of the chargers' results are presented for brevity.

In addition, each DC-DC converter is assumed to have a 3% power loss at rated condition, which is evenly distributed on its three phases. Hence, for each leg of the interleaved buck converter, a R_{loss} is added to the model in time-domain simulation, where

$$R_{loss} = \frac{360 \ kW \times 3\%}{3 \times (150 \ A)^2} = 159.9 \ m\Omega$$

3.2.1 Study System Description

The study system is based on the rural distribution feeder depicted in Fig. 1.3 and the charging station is connected to the AC bus B16 (PCC). The upstream network with respect to B16 is represented as an ideal voltage source behind a three-phase mutually coupled inductance and mutually coupled resistance model, whereas the downstream network is modeled as a balanced constant impedance load, i.e., RL, connected to the same bus; this equivalent system model adequately represents the original rural feeder and circumvents the challenge of replicating the detailed distribution system in PLECS. The model is depicted by Fig. 3.2; its parameters are summarized in Appendix A.2.1.



Figure 3.2: Charging station connected to the simplified rural distribution system.

3.2.2 Harmonic Distortion Limits

This thesis adheres to the harmonic voltage and current distortion limits provided by the IEEE 519 recommendation [61]. The recommendation specifies that for bus voltage between 1 kV and 69 kV at the PCC, maximum individual harmonic content is 3% and total harmonic distortion (THD) is 5%. Note that a THD of $\leq 3\%$ automatically satisfies both total and individual voltage harmonic limits. In contrast, the current harmonic limit is based on total demand distortion (TDD), which compares harmonic content with the peak demand load current instead of with the fundamental component as in THD. The maximum current TDD permitted based on [61] is 5% at a short-circuit ratio less than 20. The recommended maximum harmonic content for individual current harmonics and for systems with short-circuit ratios higher than 20 can be found in Table 2 on Page 7 of [61]. Among all the numbers in Table 2, the most stringent limit for TDD is 5%, for odd harmonics is 0.3%, and for even harmonics is 0.075%. Therefore, a TDD of $\leq 0.075\%$ automatically satisfies both total and individual current harmonic limits in all short-circuit ratio scenarios.

3.2.3 Short-Circuit Ratio of 6.4 at PCC

The short-circuit ratio (SCR) indicates the influence of an AC system at a specific PCC. If the AC system is relatively stiff and has a high SCR at the PCC, the amount of the PCC voltage variations will be small compared to that of a PCC with a low SCR. Hence, using SCR as a measurement of grid strength is a commonly accepted approximation, where a high SCR translates to a strong grid relative to a PCC [62].

For a load connected to a PCC, the SCR at this particular PCC is defined as

$$SCR = \frac{short - circuit \ MVA \ of \ AC \ system}{load \ MVA \ rating}.$$
(3.3)

Since this thesis considers a DC load, (3.3) becomes

$$SCR = \frac{short - circuit \ MVA \ of \ AC \ system}{load \ MW \ rating}.$$
(3.4)

Note that the short-circuit MVA is given by

$$SC \ MVA = \frac{V_{PCC}^2}{Z_{th}},$$

where V_{PCC} is the rated PCC voltage, and Z_{th} is the Thevenin equivalent impedance (assuming the AC grid can be represented by a Thevenin model).

However, in off-line simulation tools, it is easier to measure the open-circuit voltage $(V_{LL,OC})$ and short-circuit current (I_{SC}) , i.e., three-phase line-to-ground fault current, at a PCC to calculate its SC MVA using

$$SC \ MVA = \sqrt{3} \times V_{LL,OC} \times I_{SC}. \tag{3.5}$$

For the rural distribution system in Fig. 1.3, $V_{LL,OC} = 26.93 \ kV$ and $I_{SC} = 2.06 \ kA$ at bus B16, giving a SC MVA of 95.99 MVA. Since each charger is rated at 360 kW (with 3% loss) and there are three chargers in the charging station, the SCR of the rural grid at B16, which is the PCC, is calculated, based on (3.4), to be

$$SCR_{charging \ station} = \frac{95.99 \ MVA}{3 \times 1.03 \times 0.36 \ MW} = 86.3.$$

Owing to space limitations, DCFCS performance under the original rural distribution system is presented in Appendix B.2. Generally, SCR is susceptible to changes in the AC system and can vary accordingly. For example, when power lines are disconnected from the system, grid impedance increases, thereby lowering the strength of the AC grid. Hence, it is necessary to find the lowest SCR under which the charging station can remain operational, meaning it (1) is functional and (2) satisfies grid constraints, i.e., harmonics and voltage deviations.

Through comprehensive simulation case studies, the lowest SCR for the charging station to be operational is found to be 6.4 under balanced grid voltage condition, where the limiting factor in charging station operation is the PCC voltage drop.

At MROP, the total inductor current (i_t) and charging output current (i_{out}) ripples are 2.990 A and 2.950 A, respectively, as depicted in Fig. 3.3(a). This is expected since the charging current comes from the total inductor current, albeit after the output capacitor, so its ripple should be the smaller of the two. The charging output voltage (v_C) ripple, in Fig. 3.3(c), is 0.0946 V. These result in charging current and voltage percentage ripples of 3.3% and < 0.1%, respectively, which are smaller than their 5% prescribed limit. The voltage ripple is small owing to the fact that the converter terminal voltage is dictated by the battery voltage, which is relatively stiff.

The average individual phase current (i_L) ripple is 8.934 A as shown in Fig. 3.3(b). Moreover, the total inductor current and charging output current ripples have a frequency of 60 kHz and the phase current ripples have a frequency of 20 kHz. This verifies the feature of the interleaving technique where the phase current ripple has the converter switching frequency while the output current ripple has a frequency that is the number of phases multiplied by the switching frequency and the individual phase

ripple is much larger than the output ripple.

Note that the DC-link voltage, which is the input voltage for the DC-DC converter, is not constant over one VSC switching cycle and contains ripples caused by the PWM switching side-band harmonics as demonstrated by Fig. 3.3(d). This results in a low frequency (6.3 kHz) modulated envelope for the charging current and voltage.

Fig. 3.3(e) plots $|v_{PCC}|$ and demonstrates voltage drop in a realistic, non-infinite AC grid: the voltage decreased to 0.991 *p.u.* after the VSCs were activated at 0.3 second and dropped further down to 0.983 *p.u.* at MROP charging. As expected, the voltage reduction is more severe than that of the scenario with an SCR of 86.3 (Fig. B.8(e)).



Figure 3.3: Ripple content for charging at MROP: (a) Total inductor current and output charging current, (b) Phase currents, (c) Output charging voltage, (d) DC-bus voltage, and (e) $|v_{PCC}|$.

PCC voltage harmonics at MROP, except for the fundamental component, are shown in Figs. 3.4(a)

(low order harmonics, near fundamental frequency) and 3.4(b) (high order harmonics, near VSC switching frequency). The maximum PCC voltage THD is 0.136%, which is below the 3% limit. Observable harmonics include fifth, seventh components, and switching frequency side-band harmonics. PCC current harmonics other than the fundamental component for MROP are depicted in Figs. 3.4(c) and 3.4(d), where fifth, seventh components, and switching frequency side-band harmonics can be seen. The maximum PCC current TDD is 0.0981% and all of the individual even harmonics up to 120^{th} component are less than 0.01%; hence, the current harmonics are within the prescribed limit. Compared to the MROP harmonics at the scenario with an SCR of 86.3 (Fig. B.9), both voltage THD and current TDD have increased by more than two-fold as a result of weakened influence of the utility grid on PCC voltage.



Figure 3.4: PCC harmonics at MROP: (a) 2^{nd} to 29^{th} order voltage harmonics, (b) 100^{th} to 110^{th} order voltage harmonics, (c) 2^{nd} to 29^{th} order current harmonics, and (d) 100^{th} to 110^{th} order current harmonics.

At MPOP, the total inductor current, charging output current, and charging output voltage ripples become 3.072 A, 2.996 A, and 0.192 V, respectively, as shown in Figs. 3.5(a) and 3.5(c). These values give charging current and voltage percentage ripples of less than 1%, which are less than their respective values from MROP as expected. The average individual phase current ripple is 5.210 A as depicted in Fig. 3.5(b). So far, the current and voltage ripple contents for both MROP and MPOP charging conditions are very similar in both SCR of 86.3 and of 6.4 study cases, which shows that varying SCR does not affect charging ripples. At MPOP condition with a SCR of 6.4, $|v_{PCC}|$ is plotted in Fig. 3.5(e), and the voltage drop has been identified as the limiting factor. As the chargers started to supply their rated power at 0.55 second, the PCC voltage subsequently decreased to a steady-state value of 0.905 *p.u.*, which is approximately equal to the lowest steady-state voltage value of $0.9 \ p.u$. permitted by [39] and operating at MPOP below this SCR value would result in a steady-state voltage below this limit and tripping out of the DCFCS.



Figure 3.5: Ripple content for charging at MPOP: (a) Total inductor current and output charging current, (b) Phase currents, (c) Output charging voltage, (d) DC-bus voltage, and (e) $|v_{PCC}|$.

PCC voltage harmonics at MPOP, except for the fundamental component, are shown in Figs. 3.6(a) and 3.6(b). The maximum PCC voltage THD is 0.130%, which is below the 3% limit. Observable harmonics include fifth, seventh components, and switching frequency side-band harmonics. PCC current harmonics other than the fundamental component for MPOP are depicted in Figs. 3.6(c) and 3.6(d), where fifth, seventh components, and switching frequency side-band harmonics can be seen. The maximum PCC current TDD is 0.0799% and all of the individual even harmonics up to 120^{th} component are less than 0.01%; hence, the current harmonics are below the prescribed limit. Again, both voltage THD and current TDD have increased compared to their values at an SCR of 86.3 (Fig. B.11).



Figure 3.6: PCC harmonics at MPOP: (a) 2^{nd} to 29^{th} order voltage harmonics, (b) 100^{th} to 110^{th} order voltage harmonics, (c) 2^{nd} to 29^{th} order current harmonics, and (d) 100^{th} to 110^{th} order current harmonics.

Overall, the lowering of SCR did not produce any noticeable effect on charging current and voltage ripples, which is desirable, but it resulted in increases of PCC voltage THD and current TDD, albeit still much below the permitted values set by [61].

3.2.4 System Voltage Unbalance

Unbalanced grid voltages can be caused by, but not limited to, the presence of single-phase loads and unbalanced three-phase capacitor banks [63]. Several imbalance definitions exist, including the ratio of (1) the negative-sequence voltage component to the positive-sequence component, (2) maximum line-toline voltage deviation to the average line-to-line voltage, and (3) maximum phase voltage deviation to the average phase voltage [64]. The third definition is adopted in this thesis since it takes account of both negative- and zero-sequence components compared to the first definition and is easier to implement in simulation compared to the second definition.

Residential feeders often experience steady-state voltage unbalance since most loads connected to these feeders tend to be single-phase. Typical residential feeder voltage unbalance ranges between 0 and 2% [63], which is an appropriate indicator of voltage unbalance for the rural distribution system investigated in this thesis.

AC voltage unbalance is known for causing second-order harmonics in DC-link voltage, which increases charging current and voltage ripples. To reduce the 120 Hz component, a wealth of literature exists and depending on economic viability, different approaches can be considered for this problem:

- Notch filtering the DC-link voltage and VSC AC side current feedback signals to (1) synchronize to positive-sequence voltage only as in Fig. 2.3 and (2) prevent undesirable 120 Hz ripple from penetrating the control loops as in Figs. 2.4(b) and 2.4(c). Note that utilizing the 120 Hz notch filter in the VSC controller also effectively suppresses third-order harmonics in v_{sabc} and i_{tabc} [37].
- 2. Increasing the size of the DC-link capacitor.
- 3. Attenuating the 120 Hz ripple via advanced control techniques. Some well-known control schemes include dual current sequence control [37] and resonant control [65].

The first method is adopted since it has a higher affordability than the second method, is simpler to design and has a better transient response than some of the advanced control methods, i.e., dual current sequence control, and subsequent result will show that it is adequate in keeping charging ripples within their prescribed limits.

To simulate the unbalanced voltage condition, phase B voltage of the AC source is multiplied by 0.98 in order to examine the effect of the worst-case unbalance scenario on charging station operation. Note that the phase voltage can also be multiplied by a factor of 1.02; however, it would not represent the worst-case scenario as the PCC voltage is actually raised. The SCR is still kept at 6.4.

Charging at MROP, Figs. 3.7(a) and 3.7(c) show that the total inductor ripple, charging output current ripple, and charging output voltage ripple have increased to 3.094 A, 3.049 A, and 0.0979 V, respectively, resulting in charging current and voltage percentage ripples of 3.4% and < 0.1%. The average individual phase current ripple is 8.968 A as depicted by Fig. 3.7(b). The charging ripples are larger than those at balanced voltage condition owing to the presence of 120 Hz voltage distortion on the DC-bus voltage, as demonstrated by Fig. 3.7(d). $|v_{PCC}|$ is plotted in Fig. 3.7(e); it takes a sinusoidal 120 Hz waveform. Three-phase PCC line voltage and current are shown in Figs. 3.7(f) and

3.7(g). At MROP, phase B voltage is the lowest, compared to the other two phases, at 0.969 p.u. Also, the three-phase currents are more distorted than the voltages.

PCC voltage harmonics at MROP, except for the fundamental component, are shown in Figs. 3.8(a) and 3.8(b). The maximum PCC voltage THD occurs at phase B with a value of 0.137%. PCC current harmonics other than the fundamental component for MROP are depicted in Figs. 3.8(c) and 3.8(d); the maximum PCC current TDD also exists in phase B with a value of 0.0977% and all of the individual even harmonics up to 120^{th} component are less than 0.01%. Besides fifth, seventh components, and switching frequency side-band harmonics, both PCC current and voltage harmonics under unbalanced grid voltage condition contain observable third harmonic component and switching frequency component for phases A and C, which do not exist under balanced grid condition. Appearance of the third harmonics is caused by the effect of 120 Hz ripple on the control signals in dq-frame; nevertheless, owing to the use of notch filters, this harmonic component is insignificant for both voltage and current, i.e., less than $1 \times 10^{-4} p.u$. For VSC operating under balanced condition, switching frequency harmonic phase difference is not zero and the three-phase components are not annihilated, resulting in the existence of 6.3 kHz harmonics.

At MPOP, the phase B voltage dropped below 0.9 p.u. at steady-state, which is not allowed [39]. This is demonstrated by Figs. 3.9(a) and 3.9(b). Hence, the SCR limit of the charging station need to be raised in order to accommodate the 2% unbalanced condition.

Based on trial-and-error, the lowest SCR that allows the charging station to operate in worst-case unbalanced grid condition is found to be 7.1. At MPOP, the total inductor current, charging output current, and charging output voltage ripples become 3.794 A, 3.713 A, and 0.238 V, respectively, as shown in Figs. 3.10(a) and 3.10(c). These values give charging current and voltage percentage ripples of less than 1%, which are less than their respective values from MROP as expected. The average individual phase current ripple is 5.448 A as depicted in Fig. 3.10(b). Compared to operating at a SCR of 6.4, the PCC voltages did not drop below the 0.9 *p.u.* limit as shown in Figs. 3.10(e) and 3.10(f). Phase B voltage is the smallest among all three phases at MPOP with a value of $0.902 \ p.u$. Compared to MROP, the PCC current distortion is smaller since the current requirement is larger.

PCC voltage harmonics at MPOP, except for the fundamental component, are shown in Figs. 3.11(a) and 3.11(b). The maximum PCC voltage THD is 0.120% in phase B, which is below the 3% limit. Observable harmonics include third, fifth, seventh components, and switching frequency side-band harmonics. PCC current harmonics other than the fundamental component for MPOP are depicted in Figs. 3.11(c) and 3.11(d), where third, fifth, seventh components, and switching frequency side-band harmonics can be seen. The maximum PCC current TDD is 0.0585% in phase B, again below the prescribed limit. Compared to MROP at unbalanced condition, switch frequency harmonics, for both PCC voltage and current, in all three phases can be observed; this is attributed to the greater amount of current drawn at MPOP.

The charger's ability to respond to changes in reference current commands set by the EV BMS and the transition between CC and CV charging modes are investigated at the worst-case scenario, i.e., 2% unbalanced grid with an SCR of 7.1. All three chargers were simulated and had received identical EV commands; only one of the chargers' results are displayed since all three chargers' behavior were observed to be identical. Note that a current ramp limiter is implemented in the DC-DC converter's local controller with a value of 5000 A/s for (1) self-protection of the charger and (2) prolonging the EV battery's life. Only MPOP scenario is examined since it is on the steady-state operation boundary and



Figure 3.7: Waveforms for charging at MROP: (a) Total inductor current and output charging current, (b) Phase currents, (c) Output charging voltage, (d) DC-bus voltage, (e) $|v_{PCC}|$, (f) PCC three-phase line voltages, and (g) PCC three-phase line currents.



Figure 3.8: PCC harmonics at MROP: (a) 2^{nd} to 29^{th} order voltage harmonics, (b) 100^{th} to 110^{th} order voltage harmonics, (c) 2^{nd} to 29^{th} order current harmonics, and (d) 100^{th} to 110^{th} order current harmonics.



Figure 3.9: Waveforms for charging at MPOP: (a) $|v_{PCC}|$, and (b) PCC three-phase line voltages.



Figure 3.10: Waveforms for charging at MPOP: (a) Total inductor current and output charging current, (b) Phase currents, (c) Output charging voltage, (d) DC-bus voltage, (e) $|v_{PCC}|$, (f) PCC three-phase line voltages, and (g) PCC three-phase line currents.



Figure 3.11: PCC harmonics at MPOP: (a) 2^{nd} to 29^{th} order voltage harmonics, (b) 100^{th} to 110^{th} order voltage harmonics, (c) 2^{nd} to 29^{th} order current harmonics, and (d) 100^{th} to 110^{th} order current harmonics.

represents the worst-case scenario with respect to controller behavior, e.g., it causes the largest overshoot and operates near the controller saturation point.

Fig. 3.12(a) depicts charging output current after the EV BMS commanded the charger to supply 450 A at 0.55 second; prior to this event, the DC-DC converter's local controller was not activated. The current changed from 0 A to 450 A in approximately 0.095 second, roughly corresponding to the speed of the current ramp limiter, with a 1.3% overshoot of 5.64 A. Fig. 3.12(b) demonstrates the output voltage of the DCFC that increased to approximately 800 V from 771 V owing to the flow of the current into the EV battery. Isolation transformer low voltage (LV) side (VSC AC side) three-phase current and voltage are plotted in Figs. 3.12(c) and 3.12(d). Before charging had taken place, the LV side current was close to 0 A since the VSC was operating with unity power factor; the three-phase currents gradually increased as the charger began to provide power to the battery. LV side phase A current had an overshoot up to 1.057 *p.u.* at 0.648 second. The DC-bus voltage, depicted in Fig. 3.12(e), dropped to 895.46 V and recovered back to 1 kV in 0.476 second. Overall, the current and voltage waveforms at all strategic points of the fast charger are acceptable.

Afterwards, the charger was demanded to reduce its output current to 90 A, which is the minimum steady-state current the charger is designed to provide, at 1.21 seconds; the current set-point was reached in 0.072 second, with an undershoot down to 87.048 A as shown in Fig. 3.13(a). As a result of current decrease, the charger output voltage changes from 800 V to approximately 777 V as presented in Fig. 3.13(b). Transformer LV side three-phase current and voltage are plotted in Figs. 3.13(c) and 3.13(d), which show negligible fluctuations. As a result of reduced power demand from the charger, the DC-bus voltage increased to 1084.8 V and returned back to 1 kV in 0.503 second, as demonstrated in Fig. 3.13(e). Nevertheless, the voltage overshoot is still below the DC-DC converter semiconductor switches' blocking voltage value.

At 1.88 seconds, the charger was again required to supply 450 A to the EV, and the output current increased from 90 A to 450 A (shown in Fig. 3.14(a)) with an overshoot of 4.61 A within 0.0756 second, roughly corresponding to the speed of the ramp limiter. The DCFC output voltage correspondingly changed from 777 V back to 800 V as depicted by Fig. 3.14(b). Transformer LV side three-phase current and voltage are plotted in Figs. 3.14(c) and 3.14(d). The phase C current has an overshoot to $1.056 \ p.u$. at 1.959 seconds. With the increased power requirement, the DC-link voltage dropped to 909.1 V and subsequently increased to 1 kV in 0.446 second.

Lastly, Figs. 3.15(a) to 3.15(e) show charging current and voltage, transformer LV side current and voltage, and DC-link voltage, respectively, when the battery was charging at MPOP and the DCFC was commanded to transition from CC to CV mode of operation for overvoltage protection at 2.6 seconds. The output current can be observed to decrease after the command was received while the output voltage, which was increasing before 2.6 seconds, was held constant. Note in Fig. 3.15(b), the average charging output voltage has changed from 799.68 V before the transition to 799.61 V after the transition; since the local controller senses the voltage when the switching command is sent, so the measurement may be done on the ripple instead of the average value, resulting in another marginally different average voltage value after the transition. However, because the charging voltage ripple is extremely small, the change in average value is negligible. For instance, in this scenario, the change is approximately 0.07 V, less than 0.01%, and can be overlooked. Transformer LV side current and voltage can be seen to be smooth during the transition as depicted in the magnified plots on top of their respective figures. DC-bus voltage was increasing before 2.6 seconds since it was recovering from the voltage drop that was caused by the

previous load current reference change at 1.88 seconds; however, as soon as it reached 1 kV and received mode transition command at 2.6 seconds, it remained constant throughout the transition. Overall, it is clear that the mode transition is smooth and the controller was able to maintain the same voltage immediately before the request had been sent.

In summary, 2% unbalanced grid voltage with an SCR of 7.1 is found to be the worst-case grid condition, under which the DCFCS can still remain operational, in the worst-case uncontrolled charging scenario, namely, all chargers are supplying their rated power at the same time. Current and voltage waveforms in all strategic points of the charging station satisfy their requirement when operating under MPOP and MROP and also when responding to EV commands.



Figure 3.12: Current and voltage transients when charger output current changes from 0 A to 450 A: (a) Charging output current, (b) Charging output voltage, (c) Transformer LV side line currents, (d) Transformer LV side line-to-line voltages, and (e) DC-bus voltage.



Figure 3.13: Current and voltage transients when charger output current changes from 450 A to 90 A: (a) Charging output current, (b) Charging output voltage, (c) Transformer LV side line currents, (d) Transformer LV side line-to-line voltages, and (e) DC-bus voltage.



Figure 3.14: Current and voltage transients when charger output current changes from 90 A to 450 A: (a) Charging output current, (b) Charging output voltage, (c) Transformer LV side line currents, (d) Transformer LV side line-to-line voltages, and (e) DC-bus voltage.



Figure 3.15: Current and voltage transients when charger switches from CC to CV mode: (a) Charging output current, (b) Charging output voltage, (c) Transformer LV side line currents, (d) Transformer LV side line-to-line voltages, and (e) DC-bus voltage.

3.3 Performance under Faults

The performance of the charging station under three-phase line-to-line-to-ground (LLLG) and single-phase line-to-ground (LG) faults and DCFC compliance with LVRT-1 to LVRT-4 are studied. LLLG and LG faults are chosen since they represent the most severe and the most common fault scenarios, respectively. Similar to the previous section, voltage and current profiles at all strategic points for all chargers are identical; thus, results from only one of the chargers are presented.

LVRT-1 and LVRT-4 requirements are presented in Section 2.2.3; for reference, they are reproduced below:

- 1. LVRT-1: VSC should remain energized during faults with normal clearing (maximum 9 cycles) [39].
- 2. LVRT-2: VSC should provide a reactive current amounting to at least 2% of the rated current for each percent of the voltage drop within 20 ms after fault detection [40].
- 3. LVRT-3: Current overshoot of IGBTs should be limited to a maximum of 20% of the rated current.
- 4. LVRT-4: DC-bus voltage overshoot should be limited to a maximum of 20% of the blocking voltage of the DC-DC converter's power semiconductor switching devices (1.2 kV is assumed to be the blocking voltage in this thesis).

3.3.1 Study System Description

For the two study cases, the fault resistance is $0.01 \ \Omega$ and the cleared state of the fault resistance is $1 \ M\Omega$. All faults last for 0.15 second, since this is the maximum time a distributed unit is required to ride through before it is permitted to disconnected from PCC [39]; the faults clear at the first zero current crossing. Faults at the PCC are presented since they represent the most extreme results and all of the chargers were operating at MPOP immediately prior to the fault, which is the worst-case charging condition. Only worst-case grid condition was simulated, namely, 2% unbalanced grid voltage with a SCR of 7.1 at PCC.

3.3.2 Three-Phase LLLG Fault

Figs. 3.16(a) and 3.16(b) display three-phase PCC voltage and current profiles during the LLLG fault, respectively. The fault commenced at 1.23 seconds and ended at 1.38 seconds. Nonetheless, it was actually cleared at approximately 1.381 seconds for phase C, 1.383 seconds for phase B, and 1.387 seconds for phase A, at the first zero-crossings of the respective PCC currents.

The most noticeable PCC voltage excursion occurred in phase A, where the voltage reached 1.2 p.u. at approximately 1.388 seconds. However, the voltage overshoot did not exceed 1.2 p.u., which is the upper voltage limit prescribed by the NERC requirement [39]. The PCC fault currents were large owing to the small fault resistance. During the fault, phases A and C current peak values reached 8.8 p.u.; phase C current increased to 10.5 p.u. at approximately 1.235 seconds and phase B current reached -10.4 p.u. at approximately 1.238 seconds.

Transformer LV side (VSC AC side) three-phase line-to-line voltage and line current waveforms are depicted in Figs. 3.17(a) and 3.17(b). When the fault started, both voltage and current oscillated with a high frequency around 970 Hz, which are magnified in their respective subplots. Phases A and B



Figure 3.16: Waveforms during LLLG fault: (a) PCC three-phase line voltages, and (b) PCC three-phase line currents.

currents reached 3.3 p.u. and -3.1 p.u. at the beginning of the fault. Upon fault recovery, v_{AB} had an overshoot to 1.3 p.u. at around 1.388 seconds and v_{BC} reached -1.2 p.u. at around 1.384 seconds. In addition, phase B current hit 1.7 p.u. at around 1.383 seconds when the fault was cleared. Although the transformer LV side current exceeded 3 p.u. during the fault, utility transformers are able to withstand peak currents up to 4 p.u. in transient conditions.



Figure 3.17: Waveforms during LLLG fault: (a) Transformer LV side line-to-line voltages, and (b) Transformer LV side line currents.

The VSC terminal currents, i_{tabc} , did not exceed 1.2 *p.u.* throughout the fault as shown in Fig. 3.18(a), which satisfies LVRT-3. The terminal currents can be observed to first decrease at the start of the fault then subsequently increase to approximately 1 *p.u.* during the fault. The former event was caused by the de-activation of the DC-DC converter, which reduced its output current from 450 A to 0 A at approximately 1.2304 seconds, as depicted in Fig. 3.18(b). The latter event was a result of the injection of 1 *p.u.* reactive current into the AC system as a part of the fault ride-through requirement.

Figs. 3.19(a) and 3.19(b) display fault_detected flag value and $|v_{PCC}|$ (filtered), respectively. It can be observed that the fault flag indicated the fault occurrence around 1.2301 seconds as $|v_{PCC}|$ dropped to below 0.65 *p.u.* and clearance at around 1.3838 seconds as $|v_{PCC}|$ increased to 0.9 *p.u.* Note that $|v_{PCC}|$ recovered back to 0.9 *p.u.* at 1.3838 seconds, but subsequently reduced to below 0.65 *p.u.* at around 1.3851 seconds as shown in the magnified subplot. Nevertheless, owing to the two cycles delay in the fault detection mechanism as presented in Section 2.2.3, the fault flag signal did not experience



Figure 3.18: Waveforms during LLLG fault: (a) VSC terminal line currents, and (b) Charging output current.

multiple transitions.



Figure 3.19: Waveforms during LLLG fault: (a) Fault detection flag, and (b) $|v_{PCC}|$ (filtered).

Fig. 3.20(a) depicts DC-link voltage throughout the fault. The voltage decreased to 933.4 V at approximately 1.381 seconds, reached 1138.6 V at around 1.391 seconds, and eventually settled back to 1 kV at approximately 1.560 seconds. The drop in DC-bus voltage was caused by the active current, i_{td} , not reaching exactly at a value of 0 *p.u.* but with a small positive offset of around 0.0059 *p.u.*, which discharged the DC capacitor. Overall, the DC-link voltage did not exceed the blocking voltage of the DC-DC converter's MOSFET switches, which complies with LVRT-4.

 i_{tq} (filtered) and its reference profiles are presented in Fig. 3.20(b). Since $|v_{PCC}|$ dropped to below 0.5 *p.u.*, as depicted by Fig. 3.19(b), at around 1.2301 seconds, reactive current amounting to 1 *p.u.* needs to be injected to the AC system as required by LVRT-2. This was satisfied when i_{tq} reached -1 p.u. at approximately 1.2442 seconds. Once the fault was cleared, the reactive current returned to unity power factor operation and reached its steady-state value at around 1.4 seconds.

Overall, the fast chargers' VSCs were always energized and connected to the utility grid, which demonstrates that LVRT-1 is satisfied.



Figure 3.20: Waveforms during LLLG fault: (a) DC-bus voltage, and (b) i_{taref} and i_{ta} .

3.3.3 Single-Phase LG Fault

The LG fault started at 1.23 seconds on phase B, and was cleared at approximately 1.384 seconds at the first zero-crossing of the phase B current. Fig. 3.21(a) show the three-phase PCC line voltages and it can be observed that during the fault, phase voltages were not balanced. Upon fault recovery, phase B voltage reached $-1.2 \ p.u$. at around 1.385 seconds. Again, the voltage overshoot did not exceed the NERC prescribed 1.2 p.u. upper limit. PCC line currents are depicted in Fig. 3.21(b), where phase B fault current reached $-10.2 \ p.u$. at approximately 1.238 seconds. On average, phase B peak current was 8.4 p.u, phase A peak current was 4.2 p.u. and phase C peak current was 3.4 p.u. during the fault.



Figure 3.21: Waveforms during LG fault: (a) PCC three-phase line voltages, and (b) PCC three-phase line currents.

Transformer LV side voltage and current profiles are displayed in Figs. 3.22(a) and 3.22(b). When the fault commenced, v_{BC} had high frequency oscillations of approximately 830 Hz. Upon fault clearance, v_{BC} reached $-1.3 \ p.u$. at approximately 1.385 seconds. For line currents, phase B current hit $-1.8 \ p.u$. and 1.6 p.u. at around 1.231 seconds and 1.235 seconds, respectively. Phase C current reached $-1.8 \ p.u$. at approximately 1.234 seconds.

VSC current, i_{tabc} shown in Fig. 3.23(a), did not exceed 1.2 *p.u.* throughout the LG fault, complying with LVRT-3. The charging output current dropped to 0 A at approximately 1.234 seconds as depicted in Fig. 3.23(b).

Fault flag and $|v_{PCC}|$ (filtered) are plotted in Figs. 3.24(a) and 3.24(b), respectively. The flag was



Figure 3.22: Waveforms during LG fault: (a) Transformer LV side line-to-line voltages, and (b) Transformer LV side line currents.



Figure 3.23: Waveforms during LG fault: (a) VSC terminal line currents, and (b) Charging output current.

raised at 1.2338 seconds and went down at around 1.3844 seconds. Note that $|v_{PCC}|$ fluctuated outside of the hysteresis block range (0.9 *p.u.* and 0.65 *p.u.*) for approximately 15 ms since the start of the fault at 1.23 seconds; however, the fault flag did not experience multiple transitions owing to the two cycle delay in the fault detection mechanism.



Figure 3.24: Waveforms during LG fault: (a) Fault detection flag, and (b) $|v_{PCC}|$ (filtered).

DC-bus voltage is depicted in Fig. 3.25(a). The voltage first decreased to 960.3 V at approximately 1.234 seconds, which was caused by the de-activation of the DC-DC converter; then it reached up to 1248.6 V with 120 Hz oscillations during the fault. When the fault cleared, the DC-bus voltage dropped to 903.2 V before settling back to 1 kV at approximately 1.6 seconds. Since the DC-link voltage overshoot never exceeded 20% of the blocking voltage of 1.2 kV, LVRT-4 is satisfied. Fig. 3.24(b) shows that the reduction in $|v_{PCC}|$ was around 0.31 *p.u.* Fig. 3.25(b) demonstrates that i_{tq} reached $-0.62 \, p.u.$ at around 1.240 seconds, complying with LVRT-2. i_{tq} reached its steady-state unity power factor operation value at approximately 1.4 seconds.



Figure 3.25: Waveforms during LG fault: (a) DC-bus voltage, and (b) i_{tgref} and i_{tq} .

Under the LG fault, all signals exhibit double line-frequency components even though 120 Hz notch filters are used in the VSC local controller, which shows the severity of the imbalance. Overall, the DCFCS was always connected to the utility grid, satisfying LVRT-1; all voltage and current fluctuations at strategic points are inside their prescribed ranges.
3.4 Conclusions

This chapter provides the performance evaluation of the DC fast charging station under (1) AC grid with steady-state non-idealities including low SCR and unbalanced grid voltages and (2) temporary LLLG and LG faults in an off-line time-domain simulation environment. Two charging points, namely, maximum power output and maximum percentage current ripple, are investigated. Under non-ideal grid conditions, the DCFCs are able to provide charging current and transition between different modes of operation as commanded by the EV BMS, with negligible voltage and current fluctuations and charging ripples. Although the DCFC controller is designed around a nominal EV battery internal resistance of 60 $m\Omega$, R_b variation (64.125 $m\Omega$ at MPOP and 32.063 $m\Omega$ at MROP) did not affect the charging station's performance. When grid voltages are balanced, the lowest short-circuit ratio for the charging station to remain operational is found to be 6.4. In comparison, under grid with 2% voltage unbalance, the lowest SCR for operating the charging station is 7.1. In all scenarios, PCC line voltage and current harmonics are kept within their limits and PCC voltage drop is identified as the limiting factor to the charging station operation. Simulating the charging station under fault conditions reveals that the fault ride-through mechanism implemented in the DCFC VSC local controller is able to comply with LVRT-1 to LVRT-4 requirements.

Chapter 4

Performance Enhancement of the DC Fast Charging Station

Chapters 2 and 3 have provided detailed controller design and performance evaluation of the DC fast charging station. This chapter describes two ways to enhance the charging station performance so that its operational SCR can be extended down to 4.0 at 2% unbalanced grid. The first enhancement method enforces a charging power limit for each DCFC as the PCC voltage drops. The second method integrates a BESS with the charging station and proposes a supervisory control solution for the operation of the BESS-enhanced DC fast charging station (hereafter referred to as BESS-DCFCS). In this chapter, the DCFC VSC DC side is connected to an equivalent controlled current source because it is an adequate representation of the detailed DC-DC converter and EV battery models and also reduces the off-line simulation time.

4.1 Performance Enhancement without BESS

Depending on economic viability, a BESS may not be available and load curtailment, i.e., controlled charging approach, is the only option to prevent the PCC voltage from dropping below $0.9 \ p.u$. The curtailment scheme should have the following features:

- Speed: The maximum time duration the PCC voltage can stay below 0.9 *p.u.* is 3 seconds [39]; hence, the curtailment algorithm should take less than 3 seconds to compute the allocated charging power.
- Compatibility: SCR and grid voltage profile can change; in addition, the charging station can supply more power in a grid with a higher SCR value without causing the PCC voltage becoming less than 0.9 *p.u.* compared to in a grid with a lower SCR value. Thus, the curtailment strategy should be (1) functional under SCR values of 4.0 (weakest) and above, and (2) providing higher charging limits as grid voltage becomes higher, i.e., the allowable charging power cannot be always fixed to a safe number that works under all conditions.

4.1.1 Proposed Curtailment Strategy

To achieve the above-mentioned objectives, a generalized piece-wise linear curtailment scheme is proposed for each charger in a DC fast charging station that is composed of N DCFCs; the scheme is described by a function

$$h_j: |v_{PCC}| \to P_j$$

where h_j is the curtailment function for j^{th} charger (j = 1, ..., N; N = 3 in this thesis), $|v_{PCC}|$ is the PCC voltage magnitude, and P_j is the maximum output power allocated for j^{th} charger.

The function h_i is characterized by three linear segments:

$$P_{j} = \begin{cases} P_{j}^{max}, & |v_{PCC}| \ge A_{j} \\ P_{j}^{max} - \frac{P_{j}^{max} - B_{j}}{A_{j} - 0.9} \times (A_{j} - |v_{PCC}|), & 0.9 \ p.u. < |v_{PCC}| < A_{j} \\ B_{j}, & |v_{PCC}| \le 0.9 \ p.u. \end{cases}$$

where P_j^{max} is the rated power of j^{th} charger, A_j is the PCC voltage below which the maximum allowable power will be less than P_j^{max} , and B_j is the lower limit of the curtailed power. It can be seen that $B_j \leq P_j \leq P_j^{max}$. A graphical representation of h_j is shown in Fig. 4.1. The function h_j acts as an upper bound function such that a DCFC can operate anywhere below its curve.



Figure 4.1: Curtailment function h_j .

Four features are brought about by implementing such curtailment scheme for a charging station:

- 1. Ease of implementation: The curtailment curve can be easily realized by a simple look-up table (LUT) and no convoluted algorithm is involved.
- 2. Charging prioritization: By choosing A_j and A_k such that $A_j < A_k$, more power is allocated to j^{th} charger than k^{th} charger since the curtailment will take effect later for the j^{th} than the k^{th} charger. If $A_j = A_k$, then both chargers have the same priority. This result can be extended to all N chargers in the charging station.
- 3. Plug-and-play: The number of chargers is not limited and each newly installed charger can easily adopt this curtailment strategy since it is not computationally intensive.

4. Stable operating point: The curtailment scheme ensures a stable operating point can be reached and $|v_{PCC}|$ is guaranteed to stay above or equal to 0.9 *p.u.* for SCR values greater than or equal to a lower bound.

The last feature can be proved by considering the superposition of all curtailment curves as a single function, $g: |v_{PCC}| \to P_{CS}$, defined as

$$g = \sum_{j=1}^{N} h_j, \tag{4.1}$$

where P_{CS} is the maximum power that can be supplied to the charging station.

Remark 1. g is a piece-wise linear (non-strictly) increasing function; it has a lower bound value P_{LB} (that has yet to be defined) and an upper bound value P_{UB} (that is the rated power of the charging station; about 1.1 MW in this thesis).



Figure 4.2: Single-line diagram of a utility grid connected charging station.

Consider the system in Fig. 4.2 where a charging station is represented by a load labeled CS; CS is connected to a Thevenin equivalent utility grid model (AC voltage source behind an impedance Z). Let $f_X : P_{PCC} \rightarrow |v_{PCC}|$ represent the relationship between the active power drawn at the PCC, P_{PCC} (positive value indicates from source to load), and the PCC voltage magnitude, $|v_{PCC}|$, at an SCR value of X. The SCR value can be changed by varying Z. Based on Kirchhoff's Voltage Law, f_X has two properties:

- 1. It is (non-strictly) decreasing.
- 2. $f_{X_1} \ge f_{X_2}$ for $X_1 \ge X_2$.

Physically, the first property means that the PCC voltage drops as the load takes more power; the second property means that given the same load power, the PCC voltage drop in a system with a higher SCR is less than that of a system with a lower SCR.

Remark 2. The inverse of f_X , $f_X^{-1} : |v_{PCC}| \to P_{PCC}$, also satisfies the above two properties; the result follows straightforwardly from the definitions.

An assumption can be made: $f_X^{-1}(1 \ p.u.) \leq P_{UB} \ \forall X$ (supplying charging station rated power causes the PCC voltage to be less or equal to 1 *p.u.* for all SCR values).

Proposition. Let $P_{LB} \leq f_M^{-1}(0.9 \ p.u.)$ where M is the smallest SCR to be considered for the designed system (4 in this thesis), then g intersects f_X^{-1} only once for all $X \geq M$ between $0.9 \ p.u. \leq |v_{PCC}| \leq 1 \ p.u.$

Proof. Firstly, since both g and f_X^{-1} are monotonic but in reverse directions, they would have at most one intersection point. Assume that there is a f_X^{-1} such that $X \ge M$ but does not intersect with gbetween 0.9 $p.u. \le |v_{PCC}| \le 1$ p.u. This means that f_X^{-1} must be either greater than g or less than g in this voltage interval. Since $f_X^{-1}(1 \ p.u.) \le P_{UB}$, then g must be greater than or equal to f_X^{-1} at $|v_{PCC}| = 1$ p.u. Also, since $f_{X_1}^{-1} \ge f_{X_2}^{-1}$ for $X_1 \ge X_2$, then $f_X^{-1}(0.9 \ p.u.) \ge f_M^{-1}(0.9 \ p.u.) \ge P_{LB}$ and gmust be less or equal to f_X^{-1} at $|v_{PCC}| = 0.9 \ p.u.$ It follows that f_X^{-1} cannot be strictly greater than gor less than g in the interval of 0.9 $p.u. \le |v_{PCC}| \le 1$ p.u. Hence, such f_X^{-1} does not exist. The proof is visually represented by Fig. 4.3.



Figure 4.3: Visual representation of the proof.

In conclusion, the proposed approach ensures that a steady-state operating point always exists for all SCR greater than or equal to M to keep $|v_{PCC}| \ge 0.9 \ p.u$. as required by [39]. Furthermore, the charging limit is dynamic, i.e., it becomes larger when PCC voltage increases. To impose minimal curtailment at an SCR of M, P_{LB} can be set to $f_M^{-1}(0.9 \ p.u.)$. g can also be adjusted to achieve minimal power curtailment at certain SCR values that the fast charging station is expected to operate most of the time. Finally, one method to divide P_{LB} among N chargers is using their relative $(1 - A_j)$ ratios to obtain B_j , i.e.,

$$B_j = P_{LB} \times \frac{1 - A_j}{\sum_{j=1}^N (1 - A_j)}.$$
(4.2)

4.1.2 Implementation and Simulation Results

The proposed load curtailment scheme is implemented for the system depicted in Fig. 4.4 in the PLECS off-line simulation software.

In the actual implementation, $|v_{PCC}|$ (after filtered by a NF and a LPF) is passed through a moving average filter with an averaging window of 10 cycles and the LUT, as displayed in Fig. 4.5. The reason for adopting such averaging filter is to attenuate $|v_{PCC}|$ fluctuations and emulate inertia for the droop-based curtailment; the averaging window was determined experimentally as a trade-off between the speed and reaction time of the curtailment scheme.



Figure 4.4: DC fast charging station without BESS enhancement.



Figure 4.5: Actual implementation of h_j .

- Reactive power support (RPS): A hysteresis structure is implemented such that when the PCC voltage drops below 0.91 *p.u.*, i_{tqref} of the DCFC VSCs are set to 0 *p.u.* so that the VSC filter capacitors, C_f , can inject reactive power to raise the PCC voltage and consequently the curtailment limit; when the voltage returns above 0.97 *p.u.* the VSCs return back to unity power factor operation. This increases the value of f_X^{-1} on the interval of $|v_{PCC}| < 0.97$ *p.u.* and does not affect the results from the previous section.
- Intermediate voltage detection (IVD): In scenarios that cause $P_{LB} > f_X^{-1}(0.9 \ p.u.)$, i.e., SCR reduces below M, the curtailment method cannot ensure that the PCC voltage can stay above or equal to 0.9 p.u. An IVD mechanism is implemented such that if $|v_{PCC}| < 0.9 \ p.u$. for 2.5 seconds, charging station's output power will be decreased to 0 W; charging will resume when $|v_{PCC}| \ge 0.98 \ p.u$. for 0.1 second (this voltage limit is selected to indicate that the grid condition has returned to normal).

IVD is different from the fault ride-through's LVD mechanism in two aspects: i) NERC Standard specifies that the PCC voltage can remain between 0.65 p.u. and 0.9 p.u. for a maximum of 2.7 seconds [39]; the IVD mechanism actively prevents the charging station from being tripped out by the protective relay by curtailing output power to 0 W when the PCC voltage is below 0.9 p.u. for 2.5 seconds (in other words, a preemptive action); in contrast, the relay will trip the charging station when the PCC voltage drops below 0.65 p.u. for more than 0.3 second, so, in this thesis, the PCC voltage becoming less than 0.65 p.u. is treated as a fault and LVD activates in this scenario; ii) LVD takes precedence over IVD.

Note that there are other methods for handling such events and IVD is implemented as a proof of concept to demonstrate the need for such a mechanism.

Simulation Results

Charging station operation scenario 1: The charging station is operated in a 2% unbalanced grid with an SCR of 4. At 0.3 second, the VSCs were activated; at 0.5 second, all three DCFCs were ordered to supply rated power. Since all chargers received the same command and had the same power profiles, only one of the chargers' active and reactive power waveforms are displayed in Figs. 4.6(a) and 4.6(b), respectively. At steady-state, the real power flowing into the charger was approximately 374 kW. The reactive power was initial around 0 VAr (unity power factor operation). However, $|v_{PCC}|$ (Fig. 4.6(c)) became less than 0.91 *p.u.* at approximately 0.54 second and the VSC filter capacitor began injecting reactive power into the grid as commanded by RPS. At steady-state, the reactive power injection by the DCFC was approximately 47.6 kVAr. Nonetheless, even with reactive power support, the PCC voltage remained below 0.9 *p.u.* and load curtailment is required to prevent disconnection of the charging station from the grid.

<u>Charging station operation scenario 2</u>: The proposed curtailment strategy was implemented; in this study case, all three chargers had equal priorities, meaning $A_1 = A_2 = A_3 = 0.915 \ p.u$. while $B_1 = B_2 = B_3 = 308 \ kW$ (the value of B_j was determined through simulation so that the PCC voltage could stay at 0.9 *p.u*. at an SCR value of 4). Again, the charging process started at 0.5 second and the chargers were commanded to supply rated power. At steady-state, the DCFC real power was around 310 kW (Fig. 4.7(a)) and reactive power injection was approximately 56.9 kVAr (Fig. 4.7(b)). Fig. 4.7(d)



Figure 4.6: Charging station operation scenario 1: (a) Charger 1 real power profile, (b) Charger 1 reactive power profile, and (c) $|v_{PCC}|$.

Rea

PCC Voltage (p.u.)

(c)



demonstrates that all three phase voltages remained above or equal to 0.9 p.u. owing to the curtailment scheme. The result shows that the charging station grid operation limit is improved.

Figure 4.7: Charging station operation scenario 2: (a) Charger 1 real power profile, (b) Charger 1 reactive power profile, (c) $|v_{PCC}|$, and (d) PCC three-phase line voltages.

(d)

Charging station operation scenario 3: Unequal priority charging is demonstrated in this case where A_1 , A_2 , and A_3 were chosen to be 0.91 p.u., 0.92 p.u., and 0.93 p.u., and B_1 , B_2 , and B_3 were calculated based on (4.2) to be 346.5 kW, 308 kW, and 269.5 kW, respectively. All three chargers' real and reactive power profiles are depicted in Figs. 4.8(a) and 4.8(b), respectively. At steady-state, real powers for chargers 1, 2, and 3 were 349 kW, 310 kW, and 271 kW, respectively, while each charger injected approximately 57 kVAr of reactive power to the grid. This shows that charger 1 had the highest charging priority whereas charger 3 had the lowest priority. Subsequently, both chargers 1 and 2 stopped charging at 2 seconds. Hence, their active powers decreased to 0 W and charger 3 curtailed power limit was raised to 374 kW. Also, RPS was de-activated at approximately 2.04 seconds when $|v_{PCC}|$ exceeded 0.97 p.u. This set-point change indicates that the system was able to reach a new equilibrium point and the curtailment scheme did not conflict with this point since it was below the curtailment curve. $|v_{PCC}|$, displayed in Fig. 4.8(c), remained at or above 0.9 p.u. in steady-state operations.

Charging station operation scenario 4: Starting at 0.5 second, the previous non-identical priority curtailment scheme was in effect. At 1.3 seconds, a three-phase balanced resistive load of 330 kW was connected to the PCC, causing SCR to reduce to 3.8 and $|v_{PCC}|$ (Fig. 4.9(c)) to drop to approximately 0.85 p.u., which could not be recovered with the implemented curtailment function. Thus, when the PCC voltage stayed around 0.85 p.u. for 0.3 second (theoretically should be 2.5 seconds as described previously, but owing to computer hardware limitations, 2.5 seconds was too long to simulate in the off-



Figure 4.8: Charging station operation scenario 3: (a) Real power profile, (b) Reactive power profile, and (c) $|v_{PCC}|$.

line environment), the IVD mechanism disabled charging (Fig. 4.9(d)) and the PCC voltage subsequently resumed to above 0.9 *p.u.* However, the charging process was still disabled since the PCC voltage did not return to 0.98 *p.u.* which signaled that the grid condition had not been recovered. It was not until approximately 2.2 seconds when the load was removed and the voltage remained above 0.98 *p.u.* for 0.1 second that IVD enabled the charging process again.



Figure 4.9: Charging station operation scenario 4: (a) Real power profile, (b) Reactive power profile, (c) $|v_{PCC}|$, and (d) IVD mechanism command.

<u>Charging station operation scenario 5:</u> The SCR was changed to 7.1 to demonstrate the compatibility of the curtailment scheme. The same unequal priority curtailment function as in *Charging Station Operation Scenario 3* was implemented. When the chargers requested maximum power at 0.5 second, charger 1 was able to supply its rated power of 374 kW, chargers 2 and 3 real powers were curtailed to 355 kW and 312 kW, respectively (Fig. 4.10(a)). Owing to the curtailment, phase B voltage was raised to 0.910 p.u. compared to its value of 0.902 p.u. (Section 3.2.4) when operating under the same condition without curtailment.

Overall, the proposed curtailment strategy and the auxiliary RPS and IVD mechanisms were able to (1) keep the charging station operational at SCR values above or equal to 4 and (2) prevent the station from being disconnected by the protective relay at SCR values below 4. Moreover, the PCC voltage THD and current TDD were within their prescribed limits in all of the five operation scenarios.



Figure 4.10: Charging station operation scenario 5: (a) Real power profile, (b) Reactive power profile, and (c) $|v_{PCC}|$.

4.2 Performance Enhancement with BESS

The charging station's operation limit can be further extended by integrating with a BESS to form a BESS-DCFCS system. The real power of the BESS can be used for load leveling whereas the BESS reactive power injection capability can help to increase the charging power curtailment limit by raising $|v_{PCC}|$; these concepts will be demonstrated in subsequent sections.

4.2.1 BESS Parameter Selection and Local Controller Design

The power rating of the storage battery is selected to be 600 kW so that it is able to keep the PCC voltage at 0.9 p.u. at an SCR of 4 when the charging station supplies its rated power. It is assumed to have an energy rating of 1.2 MWh. Fig. 4.11 depicts the BESS connection with the rest of the AC system.



Figure 4.11: BESS connected to the rural distribution system.

A DC-DC converter, e.g., buck-boost, is often used to interface the DC side of the BESS VSC with the storage battery [66]. However, since the DC-DC converter and the storage battery characteristics are not the determining factors in this work, they are represented by an ideal voltage source of 1 kV that is connected to the VSC DC side and the VSC is modeled in detail. The step-down transformer, LC filter, and switching frequency are selected in the same fashion as in Sections 2.1 and 2.2.2. Their ratings are listed in Appendix A.4. Furthermore, the VSC local controller is designed based on methods presented in Section 2.2.3, with the sole exception of DC voltage control since it is no longer necessary. Therefore, both active and reactive powers of the BESS can be utilized for enhancing the charging station performance.

Although the actual battery characteristic is not modeled, the BESS SOC can still be approximated and calculated via the Coulomb counting/current integration method. The battery current ($i_{battery}$ in Fig. 4.11) is measured and multiplied by the DC voltage ($V_{battery}$) to obtain the instantaneous battery power $p_{battery}$:

$$p_{battery}(t) = V_{battery} \times i_{battery}(t) \ [J]. \tag{4.3}$$

The battery energy, $E_{battery}$, is

$$E_{battery} = A \times \frac{\int p_{battery}(t)dt}{3.6 \times 10^9} \ [MWh], \tag{4.4}$$

where 3.6×10^9 is the conversion factor from J to MWh and A is a multiplier for speeding up the SOC variations, which is set to 1000 in this thesis.

Lastly, the SOC is derived by

$$SOC = \frac{E_{battery}}{E_{base}} + SOC_0, \tag{4.5}$$

where E_{base} is the rated battery energy (1.2 MWh) and SOC_0 is the initial state of charge of the battery that can be set manually.

4.2.2 BESS-DCFCS Supervisory Control

A supervisory control (SC) is required to coordinate operation of the BESS and the charging station. In general, supervisory control can be categorized by energy management strategies (EMS) and power management strategies (PMS) where the former concerns with long-term energy planning and the latter provides stability and preserves viable operation of the system (through active and reactive power sharing) [67]. PMS can be further classified into continuous-time PMS (CPMS) and discrete-time PMS (DPMS) where CPMS ensures stability within one state of operation and DPMS searches for the next viable operational state when a discrete-time event takes place, e.g., BESS SOC reaching its critical limit [67]. This thesis investigates the stability and integrity of BESS-DCFCS operation; hence, both CPMS and DPMS are developed for the BESS-DCFCS system while EMS is not considered in this work.

The objectives of the supervisory control are listed below in a descending priority order:

- 1. Prevent the DC fast charging station from being tripped by the protective relay as a result of EV or BESS charging.
- 2. Keep the storage battery working in a specified SOC range to maintain its health and lifetime.
- 3. Supply maximum possible amount of power as requested by EVs, i.e., avoid on-off control.
- 4. Limit the real power supplied by the AC grid and perform load leveling.

The proposed supervisory control solution to achieve the above-mentioned objectives is shown in Fig. 4.12. The DPMS is modeled by an 11-state finite-state machine (FSM) and within each state, the BESS and the charging station operate as commanded by the CPMS. The FSM has five inputs:

- 1. SOC: The BESS SOC.
- 2. $|v_{PCC}|$: The PCC voltage magnitude.
- 3. BESS Charging: The command that initiates charging of the BESS in order to increase its SOC, which can be issued by EMS.
- 4. EV Charging: The command that indicates that the charging station is in service.



Figure 4.12: Supervisory control strategy for the BESS-DCFCS system.

5. IVD Command: The command that identifies any occurrence of low PCC voltage as a result of charging.

and two outputs:

- 1. BESS mode of operation (discussed below).
- 2. CS (charging station) mode of operation (discussed below).

The BESS operation is divided into five discrete modes; CPMS is imposed and described within each mode of operation:

• Mode of operation 1 (BESS-MO1): The BESS is used for load leveling by keeping the real power provided by the utility grid at a pre-determined level, which can be set by the utility company or EMS based on factors such as time-of-use prices. Hence, depending on the charging station's power consumption, the battery will be charged or discharged to compensate for any power mismatch.

Let P_{AC} be the amount of real power to be supplied by the AC grid, then the real power of the BESS, P_{BESS} , is set to

$$P_{BESS} = P_{AC} - P_{CS},\tag{4.6}$$

where P_{CS} is the power drawn by the charging station. As a result, i_{tdref} of the BESS VSC controller is

$$i_{tdref} = \frac{P_{BESS}}{v_{sd}}.$$
(4.7)

Note that the factor of $\frac{3}{2}$ is absent owing to the per-unitizing procedure.

The BESS reactive power is used for unity power factor operation.

- Mode of operation 2 (BESS-MO2): This mode is identical to BESS-MO1 except that a limiter is enforced on the BESS real power so that battery charging is prohibited and only discharging is allowed.
- Mode of operation 3 (BESS-MO3): The BESS real power is set to 0 W and its reactive power is used for unity power factor operation.
- Mode of operation 4 (BESS-MO4): This mode is identical to BESS-MO3 except that the BESS is allowed to charge in order to increase its SOC. The charging command and charging power set-point can be sent and determined by EMS based on factors such as time-of-use prices.
- Mode of operation 5 (BESS-MO5): This mode is identical to BESS-MO3 except that the BESS reactive power is used for LVRT AC bus voltage controller (*Q-V* droop), as described in Section 2.2.3, instead of unity power factor operation.

The charging station operation is divided into four discrete modes; CPMS is imposed and described within each mode of operation:

• Mode of operation 1 (CS-MO1): The DCFCs supply real power as demanded by the EVs and their reactive powers are used for unity power factor operation.

- Mode of operation 2 (CS-MO2): The DCFCs supply real power based on the proposed curtailment scheme and their i_{tqref} are set to 0 *p.u.* so that the VSC filter capacitors can inject reactive power to the grid.
- Mode of operation 3 (CS-MO3): This mode is identical to CS-MO2 except that the charging station output power is curtailed to 0 W.
- Mode of operation 4 (CS-MO4): This mode is identical to CS-MO3 except that the DCFCs return to unity power factor operation.

It can be seen that there are $5 \times 4 = 20$ possible operational states for the BESS-DCFCS system; however, many of these states are not permissible. Hence, DPMS is required to define a set of meaningful states of operation [67] for BESS-DCFCS depending on the system conditions and available resources:

• State 1: This state corresponds to when the BESS SOC is within its prescribed range, i.e., 20% to 80% (SOC limits should be application specific, i.e., defined based on the type of storage battery used. In this thesis, the SOC range is merely selected to demonstrate the functionality of the SC); both the BESS and the charging station operate in BESS-MO1 and CS-MO1, respectively.

If the SOC reaches its upper and lower limits, the SC switches the BESS-DCFCS system to States 2 and 3, respectively. A 2% hysteresis band is present in the actual implementation such that State 1 transitions to State 2 (or State 3) when $SOC \ge Upper\ Limit + 2\%$ (or $SOC \le Lower\ Limit - 2\%$) and returns to State 1 when $SOC \le Upper\ Limit - 2\%$ (or $SOC \ge Lower\ Limit + 2\%$).

If the IVD Command becomes non-zero, i.e., $|v_{PCC}|$ is below 0.9 *p.u.* for 2.5 seconds, State 6 will be entered.

- State 2: The BESS SOC exceeds its upper limit at this state; thus, the SC switches BESS operation to BESS-MO2 to stop further charging. State 8 will be entered if the IVD Command becomes non-zero.
- State 3: This state represents that the BESS SOC has dropped to its lower limit. Therefore, the BESS transitions to BESS-MO3 to stop further discharging. If either the BESS Charging or EV Charging command becomes non-zero, State 4 or State 5 will be entered, respectively.
- State 4: This state corresponds to BESS charging with a set-point that can be defined by EMS. Hence, the BESS switches to BESS-MO4. Note that since EV charging has a higher priority than BESS charging, if the EV Charging command becomes non-zero, the BESS will stop charging and State 5 will be entered. Finally, if $|v_{PCC}|$ becomes low, i.e., IVD Command = 1, the DPMS switches to State 10.
- State 5: This state corresponds to EV charging under low BESS SOC condition. Thus, the BESS only performs reactive power injection (BESS-MO5) and the charging station output power is curtailed (CS-MO2). State 10 will be entered if the IVD Command becomes non-zero.
- States 6 and 7: When the IVD mechanism senses that $|v_{PCC}|$ is less than 0.9 *p.u.* for 2.5 seconds, State 6 is entered and both BESS-MO5 and CS-MO3 are activated so that no charging is allowed and reactive power is injected to the AC grid to help recovering the PCC voltage. Once $|v_{PCC}| \ge$ 0.95 *p.u.*, reactive power injection is stopped while real power drawn is still zero (State 7) such

that $|v_{PCC}| \ge 0.98 \ p.u$. for 0.1 second would signal that the grid condition has returned back to normal and the charging activity can resume (State 1).

• State pairs 8 and 9 and pairs 10 and 11 are identical to pairs 6 and 7.

Note that this SC utilizes both controlled and uncontrolled charging stages, in line with current practices in the technical literature. In this thesis, SC architecture is not a focus and the controller in Fig. 4.12 is implemented in a centralized fashion. Tracing through the FSM reveals that the SC does not lead the BESS-DCFCS system into any deadlock state and transitions are meaningful with respect to the aforementioned control objectives. Four study cases are demonstrated next to verify performance of the proposed supervisory control.

Simulation Results

<u>BESS-DCFCS</u> system operation scenario 1: At 0.3 second, the system activated and since the initial SOC was 79% (Fig. 4.13(e)), the SC switched to State 1. The BESS was required to keep the real power supplied by the grid at 600 kW. Hence, initially the BESS charged with 600 kW (Fig. 4.13(a)) until its SOC reached 82% at approximately 0.53 second and the SC transitioned its mode of operation to BESS-MO2 (Fig. 4.13(d)). The BESS real power subsequently returned to 0 W. At 0.9 second, all three DCFCs started charging at rated power and the BESS discharged (negative real power as displayed in Fig. 4.13(a)) to keep the power drawn from the utility grid remain at 600 kW. Fig. 4.13(b) shows both the BESS and the charging station were operating at unity power factor mode. This operation scenario demonstrates that all three chargers could supply their rated power in a 2% unbalanced grid with an SCR value of 4 without curtailment thanks to BESS enhancement when its SOC is above the lower prescribed threshold.

<u>BESS-DCFCS system operation scenario 2:</u> This case demonstrates the transition from State 1 to State 5 when the BESS SOC dropped to 18%. Between 0.3 second and 0.5 second, the BESS charged to keep the utility power level at 600 kW (Fig. 4.14(b)); at 0.5 second, all DCFCs began drawing their maximum power (Fig. 4.14(a)) and the BESS discharged to keep grid power constant. However, the BESS SOC (Fig. 4.14(h)) decreased to 18% around 1.08 seconds and the SC consequently commanded the BESS and the charging station to operate in BESS-MO5 (Fig. 4.14(g)) and CS-MO2 (Fig. 4.14(f)), respectively. Subsequently, the BESS real power became 0 W and the DCFCs were curtailed based on the same unequal priority curtailment scheme in *Charging Station Operation Scenario 3*. At steady-state, real powers supplied to chargers 1, 2, and 3 were 374 kW, 374 kW, and 335 kW, respectively. Compared to the same scenario without the BESS (*Charging Station Operation Scenario 3*), the curtailment limits were increased owing to reactive power flow is disabled. $|v_{PCC}|$ (Fig. 4.14(e)) briefly dropped below 0.9 *p.u.* for 3.5 ms but it was within the NERC permitted range.

BESS-DCFCS system operation scenario 3: This case study starts with a low BESS SOC of 5% (Fig. 4.15(h)) and shows that the BESS was commanded to charge with 553 kW (an arbitrary amount since EMS was not implemented in this work) at 0.6 second when its mode of operation was changed to 4 (Fig. 4.15(g)). The BESS SOC subsequently increased until 1.1 seconds when the charging station began supplying its rated power; the SC immediately switched the BESS and the charging station to operate in BESS-MO5 and CS-MO2 (Fig. 4.15(f)), respectively. The BESS active power was set to 0 W and the charging station real power was curtailed. Both the BESS and the charging station also injected



Figure 4.13: BESS-DCFCS system operation scenario 1: (a) Real power profile, (b) Reactive power profile, (c) $|v_{PCC}|$, (d) BESS mode of operation, and (e) BESS SOC.



Figure 4.14: BESS-DCFCS system operation scenario 2: (a) DCFCS real power profile, (b) Grid and BESS real power profile, (c) DCFCS reactive power profile, (d) Grid and BESS reactive power profile, (e) $|v_{PCC}|$, (f) DCFCS mode of operation, (g) BESS mode of operation, and (h) BESS SOC.

<u>BESS-DCFCS system operation scenario 4</u>: In this scenario, the charging station was not supplying power and the BESS SOC was initially 5% (Fig. 4.16(e)). The BESS began charging at 0.6 second with 553 kW of active power (Fig. 4.16(a)). At 1.1 second, a three-phase balanced resistive load of 330 kW was connected to the PCC and $|v_{PCC}|$ consequently dropped to approximately 0.88 *p.u.* (Fig. 4.16(c)). The IVD Command became 1 around 1.418 seconds after the PCC voltage remained below 0.9 *p.u.* for 0.3 second (theoretically should be 2.5 seconds). Subsequently, the BESS mode of operation (Fig. 4.16(d)) switched from 4 to 5 and its active power was set to zero. The PCC voltage exceeded 0.95 *p.u.* around 1.42 seconds and the BESS began operate in BESS-MO3 (unity power factor operation). Between 1.42 seconds and the eventual load removal at 1.9 seconds, the PCC voltage stayed around 0.95 *p.u.*, which indicated that the grid condition was not suitable for enabling the BESS-DCFCS system. At 1.9 second, the load was removed, causing $|v_{PCC}|$ to become greater than 0.98 *p.u.* for 0.1 second, which signaled that it was safe to re-activate the system. The IVD Command returned to 0 at approximately 2.06 seconds, and immediately, the BESS entered charging mode (BESS-MO4) again since the BESS Charging command remained at 1 throughout this scenario; the BESS SOC began increasing again as a result.

In summary, the proposed SC is able to coordinate the BESS-DCFCS system operation under a weak and unbalanced utility grid through active and reactive power sharing by changing their respective mode of operation. The DC fast charging station's performance is enhanced through (1) real power provided by the BESS to limit the maximum power drawn by the station from the utility grid when the BESS SOC is above its lower limit and (2) reactive power injection from the BESS to raise the PCC voltage and the curtailment bound when the SOC is below its lower threshold. Moreover, the SC can maintain the BESS SOC within its prescribed range and perform load leveling to hide EV charging power fluctuations from the utility grid. Lastly, the PCC voltage THD and current TDD were within their prescribed limits in all of the four operation scenarios.

4.3 Conclusions

This chapter proposes a supervisory control solution and a charging power curtailment scheme that will enable the DC fast charging station to operate under an AC grid with 2% voltage unbalance and an SCR of 4 with and without integrating a battery storage system. The curtailment strategy is proved to be (1) functional under all SCR values equal to or greater than a designated lower bound (4 in this thesis), (2) able to allow charging prioritization if required, and (3) computationally trivial. In scenarios where SCR drops below 4, an intermediate voltage detection mechanism is implemented to stop EV charging in order to prevent the charging station from being tripped by the protective relay. The BESS is designed in line with the procedure presented in Chapter 2. Both the BESS and the charging station operations are divided into five and four discrete modes, respectively; an SC is proposed to coordinate and choose their optimal modes of operation based on the available resources and system conditions and is shown to be free of deadlock states. All operation scenarios, i.e., five scenarios for charging station operation without the BESS and four scenarios for charging station operation with the BESS, demonstrate that the above-mentioned strategies are able to (1) keep the charging station operational at grid SCR values of 4 and above in both controlled and uncontrolled charging stages, and (2) preemptively cease charging to prevent a potential disconnection from the grid when SCR becomes less than 4.



Figure 4.15: BESS-DCFCS system operation scenario 3: (a) DCFCS real power profile, (b) Grid and BESS real power profile, (c) DCFCS reactive power profile, (d) Grid and BESS reactive power profile, (e) $|v_{PCC}|$, (f) DCFCS mode of operation, (g) BESS mode of operation, and (h) BESS SOC.



Figure 4.16: BESS-DCFCS system operation scenario 4: (a) Grid and BESS real power profile, (b) Grid and BESS reactive power profile, (c) $|v_{PCC}|$, (d) BESS mode of operation, and (e) BESS SOC.

Chapter 5

Hardware-in-the-Loop Testbed for the BESS-Enhanced DC Fast Charging Station

A centralized SC was proposed for the BESS-enhanced DC fast charging station and evaluated in an offline simulation environment in Chapter 4. This chapter presents the performance of the BESS-DCFCS system implemented in a supervisory control hardware-in-the-loop (SCHIL) real-time simulation setup where the monolithic SC resides in a National Instruments (NI) CompactRIO controller and the power circuitry and its associated local controllers are modeled in the RTDS real-time simulator. In this chapter, the detailed SCHIL hardware setup is presented first, followed by a discussion on comparing the hardware-in-the-loop test with the off-line simulation, and lastly, the simulation results are given to provide an extra layer of validation for the work presented in Chapter 4.

5.1 Supervisory Control Hardware-in-the-Loop Real-Time Simulation Hardware Setup

Supervisory control hardware-in-the-loop structure adds pragmatism to the simulation because the supervisory control is implemented in a separate piece of hardware similar to a real-world setup. Thus, physical effects such as communication delay and sensor noise can be incorporated in the simulation. Another advantage of the HIL testbed is that owing to the real-time simulation, (1) the IVD mechanism's waiting time can be set to 2.5 seconds as described in Section 4.1.2 instead of 0.3 second used in the off-line simulation, and (2) the BESS SOC can be continuously varied, unlike in the off-line simulation where a new SOC_0 needs to be set to reach an operating point of interest in order to reduce simulation time.

The SCHIL interface setup is depicted in Fig. 5.1. Both the DPMS and IVD mechanisms are developed in the CompactRIO controller using LabVIEW and the BESS-DCFCS system is implemented in the RTDS platform using the RSCAD software package. The CompactRIO controller receives three analog signals from RTDS, namely, SOC, $|v_{PCC}|$, and EV Charging command; the controller has three digital outputs for binary representation of the mode of operation for the BESS (D0 to D2) and another

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Figure 5.1: Interface between the CompactRIO controller (left) and the RTDS platform (right).

three for the mode of operation of the charging station (D3 to D5), constituting a total of six digital output channels from the NI hardware to RTDS. Since IVD is also implemented in the CompactRIO controller, the IVD Command signal does not necessitate any additional input/output channel between CompactRIO and RTDS. As in Chapter 4, the BESS Charging command, which should be issued by EMS, is set by a switch on the LabVIEW's graphical user interface; the EV Charging command is set by a switch on the RSCAD's graphical user interface.



Figure 5.2: Average model representation of the BESS-DCFCS system (Chargers #2 and #3 have the same structure as Charger #1).

In the SCHIL study, the DCFC VSC DC side is connected to an equivalent controlled current source same as in Chapter 4. Furthermore, all VSCs are represented by average models, as displayed in Fig. 5.2, this is justified since (1) this chapter evaluates supervisory control performance involving changing i_{tdq} set-points in the low frequency domain and average models are adequate for this type of study, and (2) switch models have been extensively investigated in Chapters 3 and 4 which are shown to follow set-point variations with acceptable system dynamics and reiterating such results is not the purpose of the SCHIL simulation.

The local control strategy for the average model is the same as presented in Section 2.2.3 except that switching is not necessary. Neglecting switching and conduction losses, then

$$p_{AC}(t) = p_{DC}(t).$$
 (5.1)

where $p_{AC}(t)$ and $p_{DC}(t)$ are AC and DC side powers of the VSC, respectively.

Based on (5.1), the AC and DC sides of the VSC are linked via

$$i_{DC} = \frac{v_{ta}i_{ta} + v_{tb}i_{tb} + v_{tc}i_{tc}}{V_{DC}},$$
(5.2)

where v_{tabc} are *abc*-frame quantities of v_{tdq} and i_{tabc} are *abc*-frame quantities of i_{tdq} .

5.2 Comparison with PLECS Simulation

There are two major differences between the SCHIL real-time simulation and PLECS off-line simulation. The first salient distinction is the simulation time step size: PLECS uses a variable time step solver, whereas RTDS uses a fixed time step size which was set to 40 μ s for this study, as it was the smallest permitted step size on the existing hardware platform. The second dissimilarity is the usage of average models in RTDS as mentioned earlier, which eliminates high frequency dynamics compared to the results from PLECS. Hence, PCC harmonics cannot be examined. Nevertheless, since the supervisory control is only concerned with low frequency fluctuations, the modeling approach in the SCHIL real-time simulation is sufficient.

Hence, disagreements between transient results from the real-time and off-line simulations were observed even though steady-state results were similar; however, they do not affect the performance of the supervisory control and can be neglected.

5.3 Simulation Results

This section presents the real-time simulation results from seven study cases to verify the functionality of the BESS-DCFCS system as it was subjected to various continuous- and discrete-time events. All operation scenarios were simulated under a 2% unbalanced grid with an SCR value of 4. Moreover, the SOC multiplier A in (4.4) was set to 100 in the real-time simulation instead of 1000 in the PLECS off-line simulation.

BESS-DCFCS system SCHIL simulation scenario 1: Initially, the BESS SOC (Fig. 5.3(e)) was below 82% and the SC switched to State 1, where the BESS was required to keep the real power supplied by the grid at 600 kW. Hence, the BESS charged with approximately 600 kW (positive real power as displayed in Fig. 5.3(a)) until its SOC reached around 82% at 2.3 seconds. Note that the SOC did not reach precisely 82% owing to digitization error. Consequently, the SC transitioned the BESS mode of operation to BESS-MO2 (Fig. 5.3(d)) and the BESS real power returned to 0 W. The BESS SOC never exceeded 82% as a result. Compared to the same transition from *BESS-DCFCS System Operation Scenario 1* of

Section 4.2.2 simulated in PLECS, the BESS local controller in RTDS exhibited a significant negative overshoot in set-point tracking, which was caused by the large simulation time step size. Nonetheless, the difference in transient behavior did not affect the overall envelope of operation state evolution; the objective of keeping SOC at or below its upper prescribed range was fulfilled.



Figure 5.3: BESS-DCFCS system SCHIL simulation scenario 1: (a) Grid and BESS real power profile, (b) Grid and BESS reactive power profile, (c) $|v_{PCC}|$, (d) BESS mode of operation, and (e) BESS SOC.

<u>BESS-DCFCS system SCHIL simulation scenario 2</u>: At first, the BESS charged to keep the utility power level at 600 kW; at 0.2 second, all DCFCs started charging at rated power (all three chargers' profiles were identical; thus, only one charger's results are presented) and the BESS discharged (Fig. 5.4(a)) to keep grid power constant. Consequently, the BESS SOC started decreasing (Fig. 5.4(d)). Fig. 5.4(b) shows both the BESS and the charging station were operating at the unity power factor mode. This operation scenario: (1) verifies that the BESS was able to keep $|v_{PCC}|$ (Fig. 5.4(c)) at 0.9 p.u. when all three chargers were supplying their maximum power in a 2% unbalanced grid with an SCR value of 4 by providing a part of the required charging power and (2) demonstrates that the BESS-DCFCS system can be operated as a constant power load so that EV charging dynamics will not be perceived by the grid. Note that when the BESS switched to discharging around 0.3 second, a more severe negative overshoot occurred compared to the same instant from *BESS-DCFCS System Operation Scenario 2* of Section 4.2.2; as mentioned previously, this was due to the large simulation time step and did not affect the supervisory control performance result.



Figure 5.4: BESS-DCFCS system SCHIL simulation scenario 2: (a) Real power profile, (b) Reactive power profile, (c) $|v_{PCC}|$, and (d) BESS SOC.

BESS-DCFCS system SCHIL simulation scenario 3: This case demonstrates the transition from State 1 to State 5 when the BESS SOC dropped to 18%. Initially all three chargers were supplying their rated power (Fig. 5.5(a)) and the BESS discharged to keep grid power constant (Fig. 5.5(b)). However, the BESS SOC (Fig. 5.5(h)) decreased to 18% at approximately 2.4 seconds and the SC consequently commanded the BESS and the charging station to operate in BESS-MO5 (Fig. 5.5(g)) and CS-MO2 (Fig. 5.5(f)), respectively. As a result, the BESS real power became 0 W and the DCFCs were curtailed based on the same unequal priority curtailment strategy in *BESS-DCFCS System Operation Scenario 2* of Section 4.2.2. At steady-state, chargers 1, 2, and 3 provided 376 kW, 376 kW, and 340 kW, respectively; the charger active powers closely match the results obtained from the off-line simulation. Similarly, charger 2 was able to supply its rated power owing to reactive power injection from the DCFCs and the BESS as displayed in Figs. 5.5(c) and 5.5(d), respectively. $|v_{PCC}|$, as shown in Fig. 5.5(e), was within the NERC permitted range throughout the transition. The objective of keeping the SOC at or above its lower prescribed range was fulfilled.



Figure 5.5: BESS-DCFCS system SCHIL simulation scenario 3: (a) DCFCS real power profile, (b) Grid and BESS real power profile, (c) DCFCS reactive power profile, (d) Grid and BESS reactive power profile, (e) $|v_{PCC}|$, (f) DCFCS mode of operation, (g) BESS mode of operation, and (h) BESS SOC.

<u>BESS-DCFCS</u> system SCHIL simulation scenario 4: This case study demonstrates the enhancement from BESS reactive power contribution to the curtailment scheme when a resistive load of 330 kW was connected to the PCC. In *Charging Station Operation Scenario* 4 of Section 4.1.2, the same load was connected to the PCC and caused $|v_{PCC}|$ to drop to 0.85 *p.u.*, triggering the IVD mechanism. However, instead of setting the charger output power to 0 W by IVD when operating without the BESS, the chargers were curtailed to their minimum curtailment limits of 350 kW, 311 kW, and 272 kW, respectively, as depicted in Fig. 5.6(a), and the PCC voltage was kept at 0.9 *p.u.* (Fig. 5.6(c)) owing to reactive power injection from the DCFC VSCs (Fig. 5.6(c)) and the BESS (Fig. 5.6(d)). As a result, the IVD mechanism was never activated in this scenario; the BESS and the charging station were operating in BESS-MO5 and CS-MO2 throughout this scenario.



Figure 5.6: BESS-DCFCS system SCHIL simulation scenario 4: (a) DCFCS real power profile, (b) Grid and BESS real power profile, (c) DCFCS reactive power profile, (d) Grid and BESS reactive power profile, and (e) $|v_{PCC}|$.

<u>BESS-DCFCS system SCHIL simulation scenario 5</u>: In this scenario, the charging station was not supplying power and the BESS was operating in BESS-MO3 (Fig. 5.7(d)) since its SOC was at 18% (Fig. 5.7(e)). The BESS began charging at 1.64 seconds with 555 kW (Fig. 5.7(a)) when its mode of operation was changed to 4. Consequently, the BESS SOC increased as a result, as shown in Fig. 5.7(e).



Figure 5.7: BESS-DCFCS system SCHIL simulation scenario 5: (a) Grid and BESS real power profile, (b) Grid and BESS reactive power profile, (c) $|v_{PCC}|$, (d) BESS mode of operation, and (e) BESS SOC.

<u>BESS-DCFCS system SCHIL simulation scenario 6</u>: The BESS was charging with 555 kW initially, as displayed in Fig. 5.8(b), and its SOC increased (Fig. 5.8(h)) until 0.2 second when the charging station started providing its rated power, as depicted in Fig. 5.8(a); the SC immediately switched the BESS and the charging station to operate in BESS-MO5 (Fig. 5.8(g)) and CS-MO2 (Fig. 5.8(f)), respectively. The BESS active power was set to 0 W and the charging station real power was curtailed. Both the charging station and the BESS also injected reactive power to raised the PCC voltage, as shown

in Figs. 5.8(c) and 5.8(d), respectively. Similar to other SCHIL scenarios, the transition at 0.2 second had a more severe undershoot in BESS active power when BESS i_{tdref} was set to 0 *p.u.* compared to the same instant from *BESS-DCFCS System Operation Scenario 3* of Section 4.2.2, especially $|v_{PCC}|$ (Fig. 5.8(e)) had exceeded 1.1 *p.u.* for 7 ms; however, the voltage fluctuation was still within the NERC permitted standard.

BESS-DCFCS system SCHIL simulation scenario 7: This case verifies the results from BESS-DCFCS System Operation Scenario 4 of Section 4.2.2. The BESS was in BESS-MO4 (Fig. 5.9(d)) and at 1.2 seconds, the same three-phase resistive load was connected to the PCC. $|v_{PCC}|$ consequently dropped to a steady-state value of approximately 0.88 p.u. (Fig. 5.9(c)). The IVD Command became 1 at 3.7 seconds after the PCC voltage remained below 0.9 p.u. for 2.5 seconds and the BESS mode of operation was changed from 4 to 5 by the SC. Thus, the BESS active power was reduced to 0 W (Fig. 5.9(a)). 20 ms after this transition, the PCC voltage exceeded 0.95 p.u. and the SC transitioned into State 11, namely, unity power factor operation (Fig. 5.9(b)). Between 3.72 seconds and the eventual load removal at 4.2 seconds, the PCC voltage stayed around 0.95 p.u. which indicated that the grid condition was not suitable for enabling the BESS-DCFCS system. At 4.2 seconds, the load was disconnected and $|v_{PCC}|$ became greater than 0.98 p.u. for 0.1 second, causing the IVD Command to return to 0 around 4.31 seconds. The BESS entered charging mode immediately as the BESS Charging command remained at 1 throughout this scenario; the BESS SOC (Fig. 5.9(e)) began increasing again as a result.

Note that in the off-line simulation, the initial SOC has to be set to 5% in *BESS-DCFCS System Operation Scenarios 3 and 4* of Section 4.2.2 in order to reach the low SOC condition to save simulation time and memory. However, owing to the real-time simulator, the BESS SOC can be varied continuously to study the state transitions. Overall, the steady-state results from the real-time and off-line simulations match closely, but the transient results from the real-time simulation contain more severe overshoots compared to the PLECS simulation. Nevertheless, this is caused by the large time step size as mentioned above and does not affect the overall state transition envelope. It is apparent that the proposed work in Chapter 4 was able to satisfy all of the supervisory control objectives when implemented in the hardware-in-the-loop simulation environment.

5.4 Conclusions

This chapter validates the functionality of the monolithic supervisory controller for the BESS-DCFCS system. The power circuitry and its associated local controllers were implemented in the RTDS platform whereas the DPMS state-machine and IVD were realized in the National Instruments CompactRIO controller. In the off-line simulation, a variable time step solver was used and VSCs were represented by switch models. In contrast, a fixed time step solver and VSC average models were used in the real-time simulation. These two differences have created more severe overshoots in the real-time simulation results, but the overall state evolution envelope was not affected by comparing with the results obtained in Section 4.2.2. The SCHIL study proves that the proposed SC is able to satisfy all of the objectives listed in Section 4.2.2 even when non-idealities such as communication delay, sensor noise, and digitization error are incorporated in the simulation setup.



Figure 5.8: BESS-DCFCS system SCHIL simulation scenario 6: (a) DCFCS real power profile, (b) Grid and BESS real power profile, (c) DCFCS reactive power profile, (d) Grid and BESS reactive power profile, (e) $|v_{PCC}|$, (f) DCFCS mode of operation, (g) BESS mode of operation, and (h) BESS SOC.



Figure 5.9: BESS-DCFCS system SCHIL simulation scenario 7: (a) Grid and BESS real power profile, (b) Grid and BESS reactive power profile, (c) $|v_{PCC}|$, (d) BESS mode of operation, and (e) BESS SOC.

Chapter 6

Conclusions

This thesis provides an in-depth evaluation of the performance and the impact of a MW level DC fast charging station on a distribution level rural feeder. First, a fast charging station architecture is selected; then, a functional and economically viable fast charger is designed with a power rating of 360 kW. Local control strategies for the DCFC are outlined and eigenvalue sensitivity analysis is conducted to assess the impact of EV battery resistance on charger converter operation. Next, the DCFCS is tested under a wide range of grid conditions including a viable range of SCR values, unbalanced voltages, and LLLG and LG faults. Each DCFC is verified to be able to provide the requested charging current and voltage with less than 5% ripple content and remain connected to the AC grid during fault scenarios; the lowest SCR values the charging station can operate in, without violating the NERC requirement, are found to be 7.1 under 2% unbalanced grid and 6.4 under balanced grid conditions. PCC voltage drop is identified as the limiting factor to DCFCS operation, while PCC voltage and current harmonics are observed to be within the IEEE 519 recommendation under all operating conditions owing to the use of VSCs as active front ends in DCFCs.

To lower the operational SCR down to 4.0 under 2% unbalanced grid, a curtailment strategy is devised to impose a charging power limit as voltage drops in order to keep the PCC voltage greater than or equal to 0.9 *p.u.* for SCR values of 4 and above. The curtailment scheme constantly updates the charging limit with respect to voltage deviation and requires minimal computational effort. A battery storage system is also designed to enable the DCFCS to operate at SCR values of 4 and above; power management strategies are developed to coordinate the operation between the BESS and the DCFCS, which use both controlled and uncontrolled charging approaches. All studies have been conducted in the PLECS off-line simulation software and the BESS-enhanced DCFCS system is tested in the SCHIL real-time simulation environment to demonstrate the feasibility of the supervisory control for hardware implementation.

6.1 Contributions

The main contributions of this thesis work are:

• Chose and designed feasible power electronic converter topologies and local controllers for DC fast chargers with a power rating of 360 kW in a line-frequency isolation charging station architecture.

- Investigated the impact of a DC fast charging station on a distribution level power grid and identified that the bottleneck for a charging station operating in a weak grid is the PCC voltage drop.
- Proposed a load curtailment boundary for the charging station that enables charging prioritization and plug-and-play; proved that the curtailment scheme would be operational under a range of SCR values.
- Developed both continuous- and discrete-time power management strategies for a BESS-enhanced DC fast charging station such that the supervisory control can (1) prevent the charging station from being tripped by the protective relay as a result of low PCC voltage, (2) supply maximum possible amount of power as demanded by EVs, and (3) perform load leveling.

6.2 Future Works

Potential future works based on the outcomes of this thesis include:

- Optimize power electronic converter design in terms of efficiency, size, and thermal considerations; next, implement a hardware prototype of a DCFC. This would represent a convincing solution to the fast charger development.
- Study how frequency fluctuations affect the performance of the fast charging station. This is especially important if the charging station resides in an AC microgrid where most/all of the generation resources have low inertia.
- Investigate fault ride-through scenarios for the BESS-DCFCS system. As seen from fault ridethrough study cases for the DC fast charging station, the most severe transients were caused by DC-link voltage regulation before and after the faults. Since the BESS local controller does not have DC voltage regulation, the inclusion of the BESS is hypothesized not to impact the conclusion drawn from the fault ride-through results obtained in this thesis.
- Examine the impact of the curtailment scheme on system dynamic behavior, i.e., find how varying the curtailment slope will affect voltage and current overshoots and/or oscillations at strategic points.
- Instead of designing the supervisory control manually as done in this thesis, the SC should be formalized through a systematic approach, by utilizing control techniques such as Supervisory Control Theory (SCT), in order to obtain non-numerical optimal supervisory control behavior, i.e., maximally permissive, nonblocking, and correct with respect to the designer's specifications [67].
- Incorporate energy management strategies in the proposed supervisory control solution, i.e., develop optimization algorithms to determine the amount and time of EV charging and BESS charging/discharging to ensure an economical operation.
- Explore operating the BESS-DCFCS system as an AC microgrid and adding distributed generation resources in the microgrid in order to improve the charging station's reliability and resiliency. Vehicle-to-grid operations can be also incorporated.
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Appendices

Appendix A

System Specifications

A.1 DCFC VSC System Per-Unit Values

The following equations are used to calculate base values for voltage, current, and impedance given the base value for power, S_{base} :

$$V_{base} = V_{LG} \times \sqrt{2}$$

$$I_{base} = \frac{S_{base} \times \sqrt{2}}{V_{LG} \times 3}$$

$$Z_{base} = \frac{V_{LL}^2}{S_{base}}$$
(A.1)

where V_{LG} and V_{LL} are the VSC AC-side line-to-ground and line-to-line RMS voltages, respectively. In addition, the base unit values for VSC filter resistance, inductance, and capacitance can be determined from Z_{base} through:

$$R_{base} = Z_{base}$$

$$X_{base} = Z_{base}$$

$$L_{base} = \frac{X_{base}}{2\pi f}$$

$$C_{base} = \frac{1}{X_{base} \times 2\pi f}$$
(A.2)

where f is the line frequency.

Using formulas in (A.1) and (A.2), all base values for the VSC system are calculated and organized in Table A.1.

A.2 AC Grid Parameters

The overhead line, load, and transformer parameters of the rural feeder are summarized in Tables A.2 to A.4, respectively.

rabie mill rabe enarger vise system base variaes.								
S_{base}	Base value for power	0.4 MVA						
V_{LL}	Line-to-line RMS voltage	0.6 kV						
V_{LG}	Line-to-ground RMS voltage	0.346 kV						
V_{base}	Base value for voltage	0.490 kV						
I_{base}	Base value for current	0.545 kA						
Z_{base}	Base value for impedance	$0.9 \ \Omega$						
L_{base}	Base value for inductance	0.00239 H						
C_{base}	Base value for capacitance	$0.00295 \ {\rm F}$						

Table A.1: Fast charger VSC system base values.

Table A.2: Overhead line parameters.

Line Type	R1 [ohms/km]	X1 [ohms/km]	B1 [uS/km]	R0 [ohms/km]	X0 [ohms/km]	B0 [uS/km]	Summer Rating [A]	Winter Rating [A]
10ASR427	0.5523	0.4852	3.6	0.9644	1.461	1.92	321	321
40ASR427	0.2697	0.4637	4.12	0.6071	1.4052	1.86	452	452
30ASR427	0.348	0.468	3.76	0.702	1.322	0	100	100
4 ASR-48	1.3515	0.5106	3.55	1.7778	1.7066	1.72	172	172
336 AL427	0.1696	0.3809	4.33	0.4689	1.2808	1.9	655	655

Load	Load	VLL	V _{LG}	Ra	R₀	R₀	Xa	Xb	Xc	La	Lb	Lo
Name	Name	(k∨)	(kV)	(Ohm)	(Ohm)	(Ohm)	(Ohm)	(Ohm)	(Ohm)	(H)	(H)	(H)
B1	M1+M2+M3	27.6	15.9	110	109	102	36	36	34	0.096	0.095	0.089
B2	M4+M5	27.6	15.9	638	638	638	362	362	362	0.960	0.960	0.960
В3	M6	8.3	4.8	20	23	17	7	8	5	0.017	0.020	0.015
В4	M7	27.6	15.9	744	744	744	656	656	656	1.740	1.740	1.740
B5	M8	27.6	15.9	40305	40305	40305	0	0	0	0.000	0.000	0.000
В6	M9+M10 +M11+M12	27.6	15.9	1096	3216	3446	360	1057	1133	0.956	2.804	3.004
В7	M13	8.3	4.8	106	106	106				0.000	0.000	0.000
Bequivalent	M14_15_ 16_17_ 18_19_20	27.6	15.9	709	1149	622	233	378	24	0.619	1.001	0.063
B12	M21	27.6	15.9			1122			369			0.978
B13	M22+M23	27.6	15.9	4020		4824	1321		1586	3.505		4.206
B14	M24	8.3	4.8	29	31	27	10	10	9	0.025	0.027	0.023
B15	M25	27.6	15.9		2838			933			2.474	
B16	M26	27.6	15.9	24122			7929			21.031		

Table A.3: Load parameters.

Table A.4: Transformer parameters.

Transformer Name	Rating	Dhaaaa	High Voltage		L	ow Voltage	SC Impedance
	(MVA)	Phases	(kV)	Connection	(kV)	Connection	(%)
T1	3.6	3	27.6	Delta	8.3	Y0	6
T2	15	3	27.6	Y0	27.6	Y0	7.3
Т3	1	3	27.6	Y0	8.3	Y0	4
T4	3.6	3	27.6	Delta	8.3	Y0	5.65

A.2.1 Equivalent System Parameters

The positive and zero sequence impedances for the equivalent system model, which combine both source and line impedances, are displayed in Table A.5.

1		~	1	1			
Positive	Sequence	Impedance	Zero Sequence Impedance				
$R_1(\Omega)$	$X_1(\Omega)$	L_1 (H)	$R_0 (\Omega)$	$X_0 (\Omega)$	L_0 (H)		
3.011	7.123	0.0189	6.145	18.330	0.0486		

Table A.5: Upstream distribution system equivalent sequence model impedances.

Equivalently, the sequence impedance model can be translated into coupled magnetic model with the parameters shown in Table A.6.

т	abic 11.0.	opsucam	distribution system eq	urvarcine in	utuai coupi	ing model impedance	0
	Self Inductance Winding Resistance		Mutual II	nductance	Mutual Resistance		
	$X_S(\Omega)$ $L_S(\mathbf{H})$ $R_S(\Omega)$		$X_M(\Omega)$	$L_M(\Omega)$	$R_M(\Omega)$		
	10.859	0.0288	4.056	3.736	0.00991	1.045	

Table A.6: Upstream distribution system equivalent mutual coupling model impedances

Note that the relationship between the positive (R_1, X_1) and zero (R_0, X_0) sequence impedance model and the mutual magnetic coupling (X_S, X_M) between three lossy windings (R_S, R_M) model is demonstrated by the following formulas:

$$R_1 = R_S - R_M,$$

$$X_1 = X_S - X_M,$$

$$R_0 = R_S + 2R_M,$$

$$X_0 = X_S + 2X_M.$$

The parameters of phase A of the equivalent load impedance, which connects to the same bus as the fast chargers, are summarized in Table A.7. Note that since this is a balanced three-phase constant impedance load, phases B and C have the same parameters as phase A; therefore, they are not shown for brevity.

 Table A.7: Equivalent RL load parameters.

 Phase A

Phase A							
$R_{load} (\Omega)$	$X_{load} (\Omega)$	L_{load} (H)	Power Factor				
207.957	68.343	0.181	0.95				

A.3 Voltage Ride-Through Duration Curve

The curve, displayed in Fig. A.1, is reprinted from [39].

A.4 BESS Parameters

The isolation transformer steps down the voltage from 27.6 kV to 0.6 kV (line-to-line, RMS) and it is rated at 0.7 MVA. The transformer parameters are summarized in Table A.8.



Figure A.1: NERC voltage ride-through curve.

Rating (MVA)	Phases	High Voltage Low Voltage		Impedance (%)	X/R Ratio	Core Power Loss (%)		
		kV	Configuration	kV	Configuration	impedance (70)	M/It Itatio	
0.7	3	27.6	Grounded Wye	0.6	Delta	5.1	7	0.086

Table A.8: BESS isolation transformer ratings.

The BESS VSC power rating, switching frequency, and LC filter values are presented in Table A.9.

Table 11.9. DEBS VSC Tabiligs.										
Rating (MVA)	Switching Frequency (Hz)	$L_f (\mu \mathrm{H})$	$C_f \ (\mu { m F})$	Q	$r_f (\mathrm{m}\Omega)$					
0.6	6300	238.7	884.2	75	1.2					

Table A.9: BESS VSC ratings.

Appendix B

Extra Results

B.1 Performance under an Ideal Grid

The charging station is simulated under an ideal grid, meaning it is connected to an infinite AC bus, to verify the correctness of the theoretical design. Current and voltage waveforms at strategic points of the charging station are selected for demonstrating the soundness of the designed chargers.

B.1.1 Study System Description

The charging station is directly connected to a balanced 27.6 kV AC voltage source without any impedance as shown in Fig. B.1. No additional load or generation is connected to the same bus with the charger.



Figure B.1: Charging station connected to an ideal grid.

B.1.2 Ripple Content

In this section, charging output current and voltage percentage ripples are investigated, which are limited to a maximum of 5%. Note that when multiple chargers are connected to the same infinite bus, their operations will not be conflicting and the results will be identical to that of a single charger; thus, only one charger is examined and its simulation results will be representative of other chargers in the same charging station.



Figure B.2: Ripple content for charging at MROP: (a) Total inductor current and output charging current, (b) Phase currents, (c) Output charging voltage, and (d) DC-bus voltage.

Charging ripples at maximum charging current percentage ripple point (MROP) are shown in Figs. B.2(a) to B.2(d). The total inductor current (i_t) ripple is 2.978 A and the charging output current (i_{out}) ripple is 2.938 A. Also, the magnitude of the total inductor current ripple confirms the correctness of theoretical analysis in Section 2.3.2. As a result, this gives a charging output current percentage ripple of 3.3%. The individual phase current (i_L) ripples, shown in Fig. B.2(b), have an average value of 8.928 A. The DC-DC converter terminal voltage (v_C) ripple is 0.0942 V, resulting in a percentage ripple of less than 0.1%.

Charging ripples at maximum power output point (MPOP) are depicted in Figs. B.3(a) to B.3(e). Compared to charging at MROP, the larger power output in this situation caused a more pronounced DC-bus voltage ripple as demonstrated by Fig. B.3(g). As mentioned before, charging current and voltage outputs have not only 60 kHz ripples from the PWM control of the DC-DC converter, but also an envelope with a frequency of 6.3 kHz that corresponds to the switching frequency of the VSC, as indicated in Figs. B.3(a) and B.3(f). The 60 kHz ripples of total inductor current, charging output current, and charging output voltage become 2.959 A, 2.881 A, and 0.184 V, respectively. Note that

even though the charging current is smaller than the total inductor current before the capacitor, it does not conform with the calculation shown in Fig. 2.10 since the results from Section 2.3.2 does not consider the effects of DC input voltage ripples. The individual phase current ripple, depicted in Fig. B.3(c), is 5.187 A. Moreover, since the 60 kHz components vary with the 6.3 kHz envelope, it would be more meaningful to measure the range of variation between the maximum and minimum values in one cycle of this envelope in addition to the ripple in one DC-DC converter switching cycle. Considering this variation, the total inductor current, charging output current, individual phase current, and charging output voltage ripples are increased to 3.069 A, 2.993 A, 5.222 A, and 0.192 V, respectively. Nevertheless, since the output current was 450 A, the current ripple content is less than 1%. Moreover, the output voltage ripple is again negligible as the output voltage is dominantly defined by the battery.

B.1.3 Harmonic Content

In this section, since the AC bus is infinitely strong, the PCC voltage has zero harmonic content, resulting in a zero THD. Nevertheless, current harmonic distortion still needs to be evaluated by operating all three chargers in the charging station simultaneously. For all three chargers supplying maximum output powers, the three-phase current harmonics are shown in Fig. B.4(a), which plots peak magnitude against frequency. This plot depicts that the three-phase currents have a significant fundamental component, which is desirable. Fig. B.4(a) is magnified to demonstrate harmonic contents other than the fundamental: low order harmonics (near fundamental frequency) and high order harmonics (near VSC switching frequency) are shown in Figs. B.4(b) and B.4(c), respectively. Observable low order harmonics in Fig. B.4(b) include fifth, seventh, eleventh, thirteenth, and seventeenth, while zero sequence harmonics such as third and ninth are negligible. From Fig. B.4(c), the VSC switching frequency side-band harmonics centered around 6300 Hz can be seen; none of these are even order harmonics. Overall, the current TDD of each phase is 0.0690%, which is less than 0.075% and within the IEEE recommendation.

Similarly, charging at MROP resulted in a per-phase current TDD of 0.0682%, which is below the most stringent limit of 0.075%, adhering to the IEEE recommendation.

Overall, it can be observed that the charging station's PCC harmonics are less than the most stringent limits set by [61] at the two critical operating points. Thus, the ability to comply with harmonic standards is demonstrated and verified.

B.1.4 Response to EV Commands

Fig. B.5(a) depicts the current output of the DC-DC converter after it had received a command from the EV BMS to supply 450 A to the battery at 0.55 second; the converter and its local controller were not activated prior to this event. As a result, the current changes from 0 A to 450 A in approximately 0.098 second. A 1.1% overshoot of 4.75 A can be observed. Fig. B.5(b) shows the variation of charger terminal voltage, and it can be seen that the voltage increased to approximately 800 V from 771 V owing to the flow of the current into the battery. Isolation transformer LV side three-phase line currents and line-to-line voltages are presented in Figs. B.5(c) and B.5(d), respectively. Before charging had taken place, the LV side current was close to 0 A since the VSC was operating with unity power factor, and the three-phase currents gradually increased as the charger began to provide power to the battery. The maximum overshoot in phase currents occurred at phase B at 0.645 second, with a value of 0.956 p.u.. The LV side voltages stayed at 1 p.u because the AC bus was infinitely strong. The DC-link voltage



Figure B.3: Ripple content for charging at MPOP: (a) Total inductor current and output charging current with 60 kHz ripple visible, (b) Total inductor current and output charging current with 6.3 kHz ripple visible, (c) Phase currents with 60 kHz ripple visible, (d) Phase currents with 6.3 kHz ripple visible, (e) Output charging voltage with 60 kHz ripple visible, (f) Output charging voltage with 6.3 kHz ripple visible, and (g) DC-bus voltage.



Figure B.4: PCC current harmonics at MPOP: (a) DC to 120^{th} order harmonics, (b) 2^{nd} to 29^{th} order harmonics, and (c) 100^{th} to 110^{th} order harmonics.

decreased to a value of 915 V as a result of the DC-DC converter taking power from the DC capacitor, and it recovered to 1 kV in 0.5 second.



Figure B.5: Current and voltage transients when charger output current changes from 0 A to 450 A: (a) Charging output current, (b) Charging output voltage, (c) Transformer LV side line currents, (d) Transformer LV side line-to-line voltages, and (e) DC-bus voltage.

Afterwards, at 1.05 seconds, the charging current set-point was changed from 450 A to 90 A and Fig. B.6(a) depicts that the DC output current reached 90 A within 0.078 second with a 3.2% undershoot of 2.924 A. Fig. B.6(b) shows the battery terminal voltage has decreased to 776 V as a result of the charging current reduction. Transformer LV side currents and voltages in Figs. B.6(c) and B.6(d) do not exhibit any significant fluctuation, and the voltages stayed at 1 p.u. owing to the infinite AC bus. Fig. B.6(e) demonstrates the variation of VSC DC-bus voltage where it has an overshoot of 76.34 V, reaching a value of 1076.34 V, since the DC-DC converter was requesting less amount of power than when the output current was 450 A, and the DC voltage variation recovered in 0.5 second.



Figure B.6: Current and voltage transients when charger output current changes from 450 A to 90 A: (a) Charging output current, (b) Charging output voltage, (c) Transformer LV side line currents, (d) Transformer LV side line-to-line voltages, and (e) DC-bus voltage.

Lastly, Figs. B.7(a) to B.7(e) show charging current and voltage, transformer LV current and voltage, and DC-bus voltage, respectively, when the battery was charging at MPOP and the BMS commanded the charger to transition from CC to CV mode of operation for overvoltage protection at 1.75 seconds. It can be observed that the charging output current started to decrease while the charging voltage was held constant. Note in Fig. B.7(b), the average charger terminal voltage value has changed slightly before and after the transition. However, the change is approximately 0.074 V, less than 0.01%, and can be overlooked. Transformer LV side currents were also reduced, albeit not very significantly in the period shown in Fig. B.7(c). Again, transformer LV voltages in Fig. B.7(d) are always at 1 p.u. Transformer LV side current and voltage profiles are also magnified at the CC to CV transition, which are shown on top of Figs. B.7(c) and B.7(d).



Figure B.7: Current and voltage transients when charger switches from CC to CV mode at MPOP: (a) Charging output current, (b) Charging output voltage, (c) Transformer LV side line currents, (d) Transformer LV side line-to-line voltages, and (e) DC-bus voltage.

In summary, all three study cases show that the DCFC is able to respond to load reference and charging mode changes without causing significant voltage or current disturbances on both AC and DC sides.

B.2 Short-Circuit Ratio of 86.3 at PCC

Operating at an SCR of 86.3, the total inductor current and charging output current ripples, at MROP, are 2.990 A and 2.950 A, respectively, as depicted in Fig. B.8(a). The charging output voltage ripple, in Fig. B.8(c), is 0.0944 V. These result in charging current and voltage percentage ripples of 3.3% and < 0.1%, respectively. The average individual phase current ripple is 8.928 A as shown in Fig. B.8(b). Fig. B.8(e) plots the PCC voltage space phasor magnitude, $|v_{PCC}|$, calculated based on $\alpha\beta$ -frame voltages values. At 0.3 second, the VSCs were activated, and subsequently, at 0.55 second, the DC-DC converters were initialized and started charging. At MROP, $|v_{PCC}|$ reduces to 0.991 *p.u.*, which is acceptable.

PCC voltage harmonics at MROP, except for the fundamental component, are shown in Figs. B.9(a) and B.9(b). The maximum PCC voltage THD is 0.0456%, which is below the 3% limit. Observable harmonics include fifth, seventh, eleventh, thirteenth components, and switching frequency side-band harmonics. PCC current harmonics other than the fundamental component for MROP are depicted in Figs. B.9(c) and B.9(d), where fifth, seventh, eleventh, thirteenth components, and switching frequency side-band harmonics can be seen. The maximum PCC current TDD is 0.0484%, again below the prescribed limit.

At MPOP, the total inductor current, charging output current, and charging output voltage ripples become 3.068 A, 2.992 A, and 0.192 V, respectively, as shown in Figs. B.10(a) and B.10(c). These values give charging current and voltage percentage ripples of less than 1%, which are less than their respective values from MROP as expected. The average individual phase current ripple is 5.198 A as depicted in Fig. B.10(b). $|v_{PCC}|$ is plotted in Fig. B.10(e), and it can be seen that when all the chargers started to supply their rated power at 0.55 second, the voltage subsequently decreased to a steady-state value of 0.984 *p.u.*, more reduction compared to MROP, as expected. However, this drop is still allowed.

PCC voltage harmonics at MPOP, except for the fundamental component, are shown in Figs. B.11(a) and B.11(b). The maximum PCC voltage THD is 0.0461%, which is below the 3% limit. Observable harmonics include fifth, seventh, eleventh, thirteenth components, and switching frequency side-band harmonics. PCC current harmonics other than the fundamental component for MPOP are depicted in Figs. B.11(c) and B.11(d), where fifth, seventh, eleventh, thirteenth components, and switching frequency side-band harmonics can be seen. The maximum PCC current TDD is 0.0513%, again below the prescribed limit.



Figure B.8: Ripple content for charging at MROP: (a) Total inductor current and output charging current, (b) Phase currents, (c) Output charging voltage, (d) DC-bus voltage, and (e) $|v_{PCC}|$.



Figure B.9: PCC harmonics at MROP: (a) 2^{nd} to 29^{th} order voltage harmonics, (b) 100^{th} to 110^{th} order voltage harmonics, (c) 2^{nd} to 29^{th} order current harmonics, and (d) 100^{th} to 110^{th} order current harmonics.



Figure B.10: Ripple content for charging at MPOP: (a) Total inductor current and output charging current, (b) Phase currents, (c) Output charging voltage, (d) DC-bus voltage, and (e) $|v_{PCC}|$.



Figure B.11: PCC harmonics at MPOP: (a) 2^{nd} to 29^{th} order voltage harmonics, (b) 100^{th} to 110^{th} order voltage harmonics, (c) 2^{nd} to 29^{th} order current harmonics, and (d) 100^{th} to 110^{th} order current harmonics.